An Aeroflex Company

Spectrum Analyzer 2398

Maintenance Manual

AC2600

Issue 1

Contains pages for

Maintenance Manual

for

SPECTRUM ANALYZER

2398

Part number AC2600
Issue 1

Creation date 31 October 2002

Please open and fit to the supplied Ring Binder

SPECTRUM ANALYZER

2398

Printed in the UK

Manual part no. AC2600
Issue 1

31 October 2002

Contents

A brief description of each section will be found on page 9, followed by a detailed contents list starting on page 11.

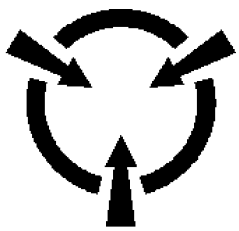
Safety Symbols

Where these symbols or indications appear on the instrument or in this manual, they have the following meanings.

WARNING. *Risk of hazard, which may cause injury to human body or danger to life. If a WARNING appears on the instruments, or in this manual, do not proceed until suitable conditions are understood and met.*

CAUTION. *Risk of hazard, which may cause fire or serious damage to the instruments or other equipment. Do not proceed until suitable conditions are understood and met.*

GROUND. *Ground terminal to chassis (earth ground).*



CAUTION. *Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).*

For Safety

WARNING ⚠

1. ALWAYS refer to the operation manual when working near locations at which the alert mark shown on the left is attached. If the operations are performed without heeding the advice the operation manual, there is a risk of personal injury. In addition, equipment performance may be reduced. This alert mark is sometimes used with other marks and descriptions indicating other dangers.

2. When supplying power to this equipment, connect the accessory 3-pin power cord to a 3-pin grounded power outlet. If a grounded 3-pin outlet is not available, and before supplying power to the equipment, use a conversion adapter and ground the green wire, or connect the frame ground on the rear panel of the equipment to ground. If power is supplied without grounding the equipment, there is a risk of receiving a severe of fatal electric shock or equipment damage.

WARNING ⚠

Repair

3. The user cannot repair this equipment. DO NOT attempt to open the cabinet or to disassemble internal parts. Only IFR trained service personnel or staff from your sales representative with a working knowledge of electrical fire and shock hazards should service this equipment. There are high-voltage parts in this equipment that present a risk of severe injury or fatal electric shock to untrained personnel. In addition, there is a risk of damage to precision parts.

Falling Over

4. This equipment should be used in the correct position, If the cabinet is turned on its side, etc., it can be unstable and may be damaged if it falls over as a result of receiving a slight mechanical shock.

For Safety

Changing the Fuses

1. Before changing the fuses, ALWAYS remove the power cord from the power-outlet before replacing the blown fuses. ALWAYS use new fuses of the type and rating specified on the fuse marking on the rear panel cabinet.

   T3.15A indicates a time-lag fuse.
   There is risk of receiving a fatal electric shock if the fuses are replaced with the power cord connected.

Cleaning

2. Keep the power supply and cooling fan free of dust. Clean the power inlet regularly. If dust accumulates around the power pins, there is a risk of fire. Keep the cooling fan clean so that the ventilation holes are not obstructed. If the ventilation is obstructed, the cabinet may overheat and catch fire.

Maximum Input

3. Maximum DC voltage ratings:

   RF Input ±20 Vdc

   Maximum AC power ratings:

   RF Input +26 dBm

   Excessive power may damage the internal circuits.

For Safety

CAUTION ⚠

Replacing Memory Back-Up Battery

4. A Primary Lithium Battery supplies the power for memory back up. A battery of the same type should only replace this battery; since IFR can only make replacement, contact the nearest IFR representative when replacement is required.

   Note: The Battery life is about 7 years.
   Early battery replacement is recommended.

Storage Medium
(PCMCIA)

5. This equipment stores data and programs using a PCMCIA (Type I) SRAM Memory Card. Trace data and Setup data may be lost due to improper use or failure. Do not remove the IC card from equipment being accessed. Isolate the card from static electricity. The back-up battery in the SRAM memory card has a limited life, replace or recharge the battery periodically.

For Safety

CAUTION !

Product Damage Precaution

6. **Use Proper Power Source:** Do not operate this product from a power source that applies more than the voltage specified.
   Provide Proper Ventilation: To prevent product overheating, provide proper ventilation.
   Do Not Operate With Suspected Failures: If you suspect there is damage to this product, have it inspected by qualified service personnel.
   Do Not Attempt To Operate If Protection May Be Impaired: If the instrument appears damaged or operates abnormally, protection may be impaired. Do not attempt to operate the instrument under these conditions. Refer all questions of proper instrument operation to qualified service personnel.

Place-related Warning

7. **Object and Liquid Entry :** Never push objects of any kind into instrument through openings as they may touch dangerous voltage points or short out parts that could result in a fire or electric shock. Never spill liquid of any kind on the instrument. Do not use this instrument near water (for example, near a bathtub, wash bowl, kitchen sink, or laundry tub, in a wet basement, or near a swimming pool). Keep the instrument away from damp air, water and dust. Unexpected trouble may be caused when the instrument is placed in a damp or dusty place.
   Flammable and Explosive Substance: Avoid using this instrument where there are gases, and where there are flammable and explosive substances in the immediate vicinity.
   Unstable Location : Do not place this instrument on an unstable cart, stand, tripod, bracket, or table. The instrument may fall, causing serious injury to a person, or serious damage to the instrument. Do not place or use the instrument in a place subject to vibration.

IFR Contact

If this equipment develops a fault, contact the head office of IFR at the address in the operation manual, or your nearest sales or service office.

Front Panel Power Switch

To prevent malfunction caused by accidentally pressing the front power switch, this equipment turns off the power if the front power switch is pressed and held for more than 1 second in the power-on state.
In the power-on state, if power is removed, then reapplied, the unit will not be turned on. Also, if there is a momentary power supply interruption or power failure, the unit will not turn on automatically. This is because this equipment enters the standby state and prevents incorrect data from being acquired when the line has to be disconnected and reconnected.

For example, if the sweep time is 1,000 seconds and data acquisition requires a long time, momentary power supply interruption (power failure) might occur during measurement and the line could be recovered automatically to power-on. In such a case, the equipment may mistake incorrect data for correct data without recognizing the momentary power supply interruption.

If this equipment enters the standby state due to momentary power supply interruption or power failure, check the state of the measuring system and press the front power switch to restore power to this equipment.

Further, if this equipment is built a system and the system power has to be disconnected then reconnected, the power for this equipment must also be restored by pressing the front power switch.

DETECTION MODE

This instrument is a spectrum analyzer, which uses a digital storage system. The spectrum analyzer makes level measurements in frequency steps obtained by dividing the frequency span by the number of measurement data points (501). Because of this operation, it is desired to use the following detector modes associated associated with appropriate measurement.

Measurement	**Detector mode**
Normal signal	POS PEAK
Random noise	SAMPLE OR AVERAGE
Pulsed noise	NORMAL
OCBW or ACP (for analog communication systems)	SAMPLE
OCBW or ACP (for digital communication system)	POS PEAK or SAMPLE

When a detection mode is specified using one of the measurement methods, make the measurement in the specified detection mode.

PREFACE

SCOPE

This manual contains maintenance instructions for the IFR 2398 Spectrum Analyzer.

The information in this manual enables servicing technicians to:

- Test or replace any major assembly within the 2398 Spectrum Analyzer.
- Maintain operating conditions of the 2398 Spectrum Analyzer to the expected performance standards.
- Understand principle of operation, relating to the overall operation of the 2398 Spectrum Analyzer as well as functional operation within the major assemblies.

ORGANIZATION

This Maintenance Manual is composed of the following sections:

<u>SECTION 1 – INTRODUCTION</u>

Provides a brief description of the electrical and mechanical configuration of the 2398, intended to familiarize the technician with the overall structure of the instrument.

<u>SECTION 2 – THEORY OF OPERATION</u>

Describes how the 2398 operates on three levels of complexity: system level, interactive functional level and functionally at the module (assembly) level.

<u>SECTION 3 – ADJUSTMENT</u>

Provides step by step procedures for calibrating the 2398.

<u>SECTION 4 – FAULT DIAGNOSIS</u>

Contains information for diagnosis of faults on the 2398.

<u>SECTION 5 – REPLACEMENT PROCEDURES</u>

Provides step by step procedures for removing and installing major assemblies within the 2398.

<u>SECTION 6 – PREVENTIVE MAINTENANCE</u>

Contains routine instructions for cleaning and inspecting the 2398.

<u>SECTION 7 – PARTS LIST</u>

Provides drawings with part listings for ordering replaceable parts within the 2398.

<u>APPENDIX</u>

Contains useful supplementary data and test equipment information.

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TABLE OF CONTENTS

Section 1

Introduction

SECTION 1
INTRODUCTION

TABLE OF CONTENTS

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SECTION 1. INTRODUCTION

General

This section contains a brief description of the internal electrical and mechanical configuration of the spectrum analyzer, providing the technician with an overall view of the product structure.

Electrical Description

The 2398 Spectrum Analyzer is microprocessor controlled. Each unit synthesizes accurate digital representations of received modulated RF signals. Accepted input frequencies range is from 9kHz to 2.7GHz.

Electronic assemblies in Spectrum Analyzer are as follows.

RF Module Assembly
IF Filter and Amp. Assembly
Video Detector Assembly
Processor Assembly
Motherboard Assembly
LCD Inverter Assembly
Keyboard Assembly
Medium Stability Oscillator Assembly
LCD Assembly
AC Power Assembly
DC Fan Assembly
Speaker Assembly
PCMCIA Card Assembly (Option)
QP Detector Assembly (Option)
GPIB Assembly (Option)
Tracking Generator Assembly (Option)
High Stability Oscillator Assembly (Option)
AC/DC Power Supply Assembly (Option)

Mechanical Description

Rear panel
Can Cover assembly
Front panel assembly
Front frame assembly
RF module assembly
IF module assembly
Video detector assembly
Processor assembly
LCD inverter assembly
Keyboard assembly
Input protect assembly
MSO/HSO assembly (Option)
LCD module assembly
AC power supply assembly
DC fan assembly
Speaker assembly
PCMCIA assembly (Option)
GPIB interface assembly
Tracking generator assembly (Option)

Section 2

Theory of Operation

SECTION 2
THEORY OF OPERATION

TABLE OF CONTENTS

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SECTION 2. THEORY OF OPERATION

General

This section provides the service technician with unit operation concepts for the 2398 Spectrum Analyzer. Theory of operation is divided into three subsections with each level more detailed in explaining actions performed within the unit.

The subsections are:

- System theory of operation

  System theory provides a simplified explanation of the overall unit function.
- Functional Theory of Operation

  Functional theory describes the signal path during each basic operation, listing the general effects the different modules have on the signal and details the different modules involved.
- Module Theory of Operation

  Module Theory explains the process in each module to functional block level. Dependencies on other modules and signal manipulation in the module are described at a functional level.

System Theory of Operation

The synthesized, phase locked 2398 Spectrum Analyzer has a frequency range up to 2.7 GHz. The microprocessor-controlled unit incorporates high-speed digital hardware to provide a wide video bandwidth for the internal display.

System Contents:

The RF Receiver block assembly is a superheterodyne type receiver with three conversions. The RF block converts the signal from the RF input connector (9 kHz to 2.7 GHz), to a 10.7 MHz IF. All controls and L.O. signals necessary for this down-conversion are contained completely within the RF Receiver block assembly.

The 10.7 MHz IF board provides the resolution bandwidths (300 Hz to 3 MHz) and IF gain necessary for the analyzer to operate.

The Video board assembly converts the 10.7 MHz signal from the IF board to a selected logarithmic or linear detected video signal. The Video board assembly also demodulates the 10.7 MHz signal to either AM or FM audio. Also included on this board is the circuitry necessary for the Frequency Counter function. After the 10.7 MHz signal is detected or demodulated, this analog video signal is then routed to the System Processor board assembly.

The System Processor board then digitizes the analog video signal to be displayed on the screen. After the video is processed, it is stored in system memory which consists of DRAM, Flash memory and SRAM backed up by the Primary Lithium battery. Also, stored in memory is the calibration and configuration data. The processor board also provides all digital controls to each assembly, sweep information to the RF block, peripheral controls (e.g. GPIB, RS-232…), digital video information to the LCD display and keyboard control. All system functions are controlled by the system software which resides on the flash RAM chip installed in the socket.

System Theory:

The 2398 receives a signal through the RF input connector. The receiver assembly in the RF block provides attenuation and down converts the intermediate frequency signal to 10.7MHz IF. The IF Filter and Amp Assembly provide the resolution bandwidth filter and IF gain for the Video Detector Assembly. The Video Detector Assembly converts the 10.7 MHz IF signal to a relative dc voltage, Video, from logarithmic, linear or demodulation detectors. The Video signal is then applied to the processor assembly. The Processor assembly digitizes the Video signal and passes the digitized information the Digital Signal Processor and System Control Microprocessor for display on the LCD assembly.

Functional Theory of Operation

Spectrum Analyzer

Front panel control settings are input to the processor assembly, determining the start frequency for the spectrum sweep. The start frequency settings are controlled by the processor assembly and locked by the phase locked loop(PLL) in the synthesizer assembly in the RF module. The processor assembly controls the synthesizer to generate the correct LO frequency for the selected Frequency Span.

The sweep mode has four modes dependent on the Frequency Span as follows.

1) DDS (Direct Digital Synthesizer) Sweep (≤ 4 MHz SPAN)
2) DDS Relock Sweep (4MHz < SPAN ≤ 10MHz)
3) Ramp Sweep (SPAN>10MHz and Sweep Time <20 sec)
4) Relock Sweep (Sweep Time ≥ 20 sec)

When the sweep mode chosen is the Ramp Sweep, the ramp signal is applied to the YIG driver circuit after the YIG is locked to the start frequency. The amplitude of ramp signal is controlled by the frequency span. The width of ramp signal is controlled by the sweep time. The other sweep mode is called digital sweep mode because the YIG is locked during sweep and controlled by the Processor Assembly.

The Input Protection Assembly provides protection from high levels instantaneous RF signals, as well as DC voltages.

The receiver assembly attenuates (0 to 50 dB) external signals coming through the Input Connector, according to Input Attenuator Control settings. In the first conversion, the input signal mixes with 3.4 to 6.1 GHz from the YIG based first L.O. and is filtered to obtain 3410.7 MHz output. In the second conversion, the 3410.7 MHz signal mixes with 3200 MHz signal generated by multiplying 80 MHz reference signal, and is filtered to obtain 210.7 MHz output. In the third conversion, The 210.7 MHz signal mixes with 200 MHz signal generated by multiplying the 80 MHz reference signal and filtered to obtain the 10.7 MHz IF signal. This signal is applied to the Resolution Bandwidth filter and amplifies the signal according to the Reference Level control settings. This signal is applied to the Video Detector Assembly for logarithmic or linear detection (controlled by the Processor Board) and is filtered and amplified in preparation for digitizing. The Processor Assembly converts the signal to digital at 200 kHz rate and the DSP processes the raw data according to the Detector Mode. The processed data is display on the LCD assembly.

RF Module Assembly

The receiver and synthesizer assemblies are included in the RF module.
The receiver assembly is a superheterodyne receiver with 3 converters.

GaAs FET Switches

The GaAs FET switches are SPDT, low insertion loss, high level switches that are intended to be used in a T/R applications. Because of the high power levels in these applications the insertion loss tends to be lower than normal to minimize dissipation in the switch itself. These switches are used in the input attenuator of the receiver.

Attenuator Pads

The attenuator pads are designed to have very good frequency response, well beyond 2.7 GHz, of less than +/-1.5 dB (after calibration). The input attenuator pad was selected to have good frequency response and attenuation accuracy in addition to being able to handle power dissipation.

Input Low Pass Filter

The RF input filter provides optimum performance and isolation. It is necessary to have very good isolation to prevent 1st LO leakage at the RF Input Connector. This is achieved by having sufficient poles in the low pass filter as well as the proper selection of the RF input and IF frequencies. In this converter the highest RF input frequency is 2.7 GHz and the center of the first IF is 3410.7 MHz. This provides additional rejection because the 1st LO is operating from 3410.7MHz to 6110.7MHz which is well into the stopband of the RF input low pass filter. The remainder of the LO leakage must be provided by good isolation and shielding of the low pass filter components. The second purpose of the RF low pass filter is for image signal rejection.

RF Preamp 1st Mixer and 1st IF Filter

The RF preamp improves the sensitivity by lowering the system noise floor. The 1st mixer is a double balanced mixer for mixing with the YIG oscillator signal. The 1st IF filters are interdigital microstrip filter which reject undesired signals. The first mixer circuit also incorporates a mixer null circuit which improves the noise performance at low RF input frequencies below 100kHz.

2nd Converter

The second converter consists of a double balanced mixer of the same type using as the 1st mixer. This is because the 2nd mixer is still operating at microwave frequencies. The 2nd LO is 3200 MHz and the RF input is the same as the 1st IF frequency of 3410.7MHz. The second IF output of 210.7MHz was chosen to permit a high performance lumped element bandpass filter to be used. The 210.7 MHz IF Bandpass Filter has a bandwidth of a approximately 6MHz and a stopband rejection of more than 90dB. This is sufficient to eliminate spurious products from appearing at the output of the 2nd IF converter.

3rd Converter

The third converter consists of a double balanced mixer, a 15 MHz low pass filter and a 3rd IF amplifier. The 15MHz low pass filter eliminates remaining spurious products from appearing at the 10.7MHz IF output and being amplified by the 10.7 MHz IF amplifier. The synthesizer assembly generates all LO's and clock frequencies for the RF module and sends those signals to the receiver assembly.

Module Voltage Regulation

The module is fed by the +15V,-15V,+5V and +24V. The +24V is used only for the YIG heater. The +15V,-15V and +5V are filtered upon entering the module by pi filters to reduce power supply noise. Some other regulator circuits are used to provide low noise voltage regulation for the lock loop oscillators.

Reference

The reference for the module is generated by a 80MHz crystal oscillator. The crystal is a 3rd overtone series resonant type. The crystal is pulled onto frequency by the series resonant circuit consisting of a varactor and inductor. This allows the crystal to operate on series resonance but still be pulled in both directions. The external medium stability oscillator is used to provide greater stability than the RF module oscillator alone. When the medium stability oscillator is connected to the RF module, the 80MHz reference is locked to the medium stability oscillator. Also, an optional high stability oscillator can be used for an ever more accurate time base. A calibration signal at 40MHz is generated for the divider chain. To provide input level calibration, the calibration, the calibration signal can be turned on and switched into the front end of the receiver.

400/200 MHz Multiplier Chain.

The 80 MHz form the reference oscillator is amplified and split by a resistive splitter. One output goes to the x5 multiplier, the other becomes the signal for the PLL return path divider chain. The multiplication is achieved by overdriving a darington MMIC which provides ample odd-order harmonics. Two stages of 3 pole helical filters are used to reject unwanted harmonics. The output of the last 400 MHz filter is again split. One signal is amplified and runs to the 3200MHz multiplier chain on the receiver assembly. The other signal is divided by 2 to generate 200MHz. The 200MHz is filtered to reduce harmonics and again split. The 200MHz signal are used for the 3rd converter LO and as a harmonic mixer injection for the clean loop synthesizer.

3200MHz Multiplier Chain.

The 3200 MHz second LO is derived from 400MHz multiplied by 8. Three stages of interdigital bandpass filters are used to reject unwanted harmonics. Each stage is isolated by a amplifier.

Synthesis Method/Frequency Scheme.

The unit uses a YIG oscillator to provide the 1st LO signal, which is the only variable frequency in the receiver. The synthesis scheme for the unit consists of 3 main chain items. The YIG oscillator is locked to a variable comb frequency in about 80MHz steps. Circuit output signal is made to cover the entire desired frequency range by providing a variable offset to the 80MHz steps. The frequency offset is variable from 0.5 MHz to 4MHz in very small increments using a direct digital synthesizer. The comb frequency signal is generated by 2 phase locked loops, the Step loop and the Clean loop.

DDS/Main Loop

The DDS operates by accessing a cosine look up table at variable rate, which is programmable. The DDS is loaded serially from the Processor assembly. The output is filtered by an LC bandpass filter. The signal is then routed back into the DDS chip which has a high speed comparator which converts the level to TTL. The output of the comparator is divided to control the spurious output of the DDS in the system. The main loop takes the DDS output and the output signal from the comb circuitry to phase lock the YIG oscillator. A discrete tri-state phase comparator is used and an integrator loop filter sets the loop bandwidth and damping factor. An out of lock indication is generated by integrating the pulsewidths from the phase detector. The loop filter contains a special circuit called the kicker circuit which keeps the phase lock away from the image response of the comb IF signal during acquisition. The comb IF frequency is about 0.5 MHz to 4MHz. If the YIG frequency is below the multiplied-up comb frequency by more than 4 MHz an image condition will occur which will result in a phase inversion in the main loop. The main loop go to its voltage limit will. The kicker circuit is a comparator with a large amount hysterisis which detects this rail condition and switches the tuneline voltage over to the comparator’s other state; which places the YIG frequency above the image. So, the main loop will usually lock from the high side.

Step Loop

The Step loop synthesizer determines in a large part the phase noise, residual noise and lock times of the all overall synthesis scheme. It runs with a reference of 400 kHz and a loop bandwidth of approximately 1.5kHz. The loop bandwidth is a compromise between switching speed and phase noise performance. The step loop oscillator runs from 180-185kHz with a tuning voltage of 4-10V. The VCO is a collector to emitter feedback design with a transistor capacitor multiplier regulator on the collector to reduce AM to PM effects.

Clean Loop

The Clean loop is an offset tracking loop. The lean loop tracks the divide down step loop. Its bandwidth is wide which allows it to track out the noise of the 660Mhz oscillator, reducing the requirements of this oscillator. The 660MHz oscillator is a tuned line collector to emitter feedback design. A microstrip element is used as the inductance for the tank circuit which maintains the Q factor needed at 660MHz.

Sweep Circuit

The sweep circuit consists of variable level ramp generator, an attenuator and switching circuitry. The ramp generator consists of a ripple counter which is triggered by a gating signal and drives a parallel multiplying D/A converter. The counter normally runs 0 to 4000 at whatever rate is coming in on the sweep clock which controls the sweep rate. The D/A reference input is driven by a 12bit DAC (SPAN DAC) which controls the output level of the ramp generator. The attenuator consists of CMOS switches and resistor dividers to generate the standard span settings. This provides the dynamic range and accuracy needed for the sweep which is unavailable using the SPAN DAC alone. The attenuator dividers are buffered to eliminate variation due to the CMOS switch impedance. Low drift resistors are used to eliminate temperature calibration on the attenuator.

Main YIG Driver

The main YIG driver consists of a high current driver, coarse tune DAC, and switching and summing circuitry for injecting a sweep signal into the main coil. In addition dual mode switching is employed to improve switching times while maintaining noise bandwidth performance. The main driver uses a voltage to current feedback loop to provide high current drive to the main coil with low noise. The sensitivity on the main coil lines is on the order of 1 GHz per volt. Three switches are used to set time constants for low noise or high speed conditions. A fixed current is summed into the main driver because the YIG requires a certain offset current. Software is used to compensated for thermal change. Low temperature coefficient resistors are used in several places to control the amount of drift over temperature range. This is due to the extremely high sensitivities of this part of the circuit.

Hold/FM YIG Driver

The Fm driver incorporates a current control loop, lock/sweep switch and an infinite hold circuit. The current loop converts voltage input to a current required by the YIG coil. The sweep, lock and hold circuits are combined in summing amplifiers to provide the correct levels at the coil. There is also a 2 pole low pass filter on the lock input to reduce reference spurious levels. The infinite hold circuit is a A/D followed by a DAC which is adjusted to be unit gain. The lock voltage is sampled, and the lock/sweep switches set to sweep which opens the tune voltage from the PLL and places the fixed voltage can be held indefinitely and will not change.

IF Filter and Amp Board Assembly

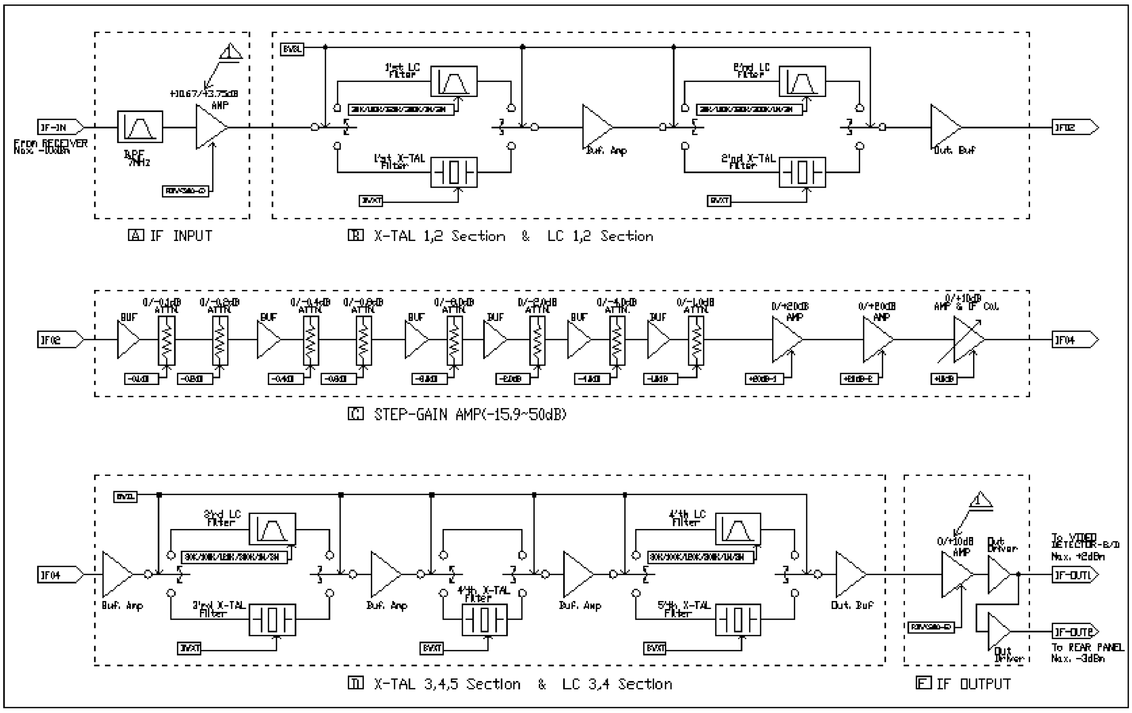

Fig. 2-1

Overview

IF Filter-Board (A3) receives the 3rd IF (10.7MHz) from the Receiver Board (A2), sends it to the Video Detector-Board (A4) and Rear-panel. The two main function of this block (A3) are as follows.

The first function is RBW (Resolution Bandwidth) filtering, which determines the frequency resolution of the Spectrum Analyzer. This defines the bandwidth and selectivity of the analyzer. RBW filters are composed of LC Filters and Crystal Filters. LC Filters provide realizes relatively wide bandwidth filters, which are 3 MHz, 1 MHz, 300 kHz, 100 kHz, 30 kHz, and 120 kHz (QP only). These RBW filters are selected by the PIN diode. In the LC Filter Mode BWSL control voltage is approximately +14 Vdc. Crystal Filters provide relatively narrow bandwidth filters, which are 10 kHz, 3 kHz, 1 kHz, 300 Hz, and 9 kHz (QP only). These RBW filters are selected by the PIN diode. In the Crystal Filter Mode, the BWSL control voltage is approximately 0 VDC.

The second function is Step-Gain amplifier, which enables the Reference Level of Spectrum Analyzer to be properly set. The IF Gain range is -15.9 dB to +50.0 dB, with 0.1 dB resolution. This block is composed of a 10 dB Step Amplifier and a 0.1dB step attenuator. A desired Reference Level is set by the appropriate mixing of the amplifier, attenuator and the input 10dB Step Attenuator of Receiver (A2).

IF Input

The +10dB Input Amplifier functions as a non-inverting op amp. In the LC Filter Mode, the current source Q3 is turned off as the voltage of BWSL line is +14 Vdc. The current of this Q2 emitter is 20 mA. About 4 mA is supplied for Q1 and 16 mA for the BWSL through CR1 and R8 in parallel with R9. In the Crystal Filter Mode, the amplifier includes Q3. In this case Q3 is turned on and the voltage of BWSL line is 0 Vdc. The current of this Q2 emitter is 20mA. About 4mA is supplied for Q1 and 16mA for Q3.

RBW Filter

The RBW filters consist of buffering amplifiers and RBW Filters. The LC Filter (wide band) have 4 stages and the Crystal Filter (narrow band) have 5 stages.

(1) Buffer Amp

The unity gain Buffer Amp functions as a noninverting op amp. The operation of this block is very similar to the IF Input amplifier block other than gain.

(2) Out Buffer

The Output Buffer Amplifier is a complementary pair of transistors in which Q9 (Q35) act as a source follower boosted by Q10 (Q36). The current through FET Q9 (Q35) is set by the parallel combination of the following resistors R75, R76, R77 (R257, R258, R259). The total current through Q9 (Q35) and Q10 (Q36) is set by the parallel combination of the following resistors R75, R76, R77 (R257, R258, R259). The input is selected by the BWSL signal from either CR16 (CR54) in the LC mode or CR19 (CR57) in the crystal mode.

(3) LC Filters (1st, 2nd, 3rd and 4th)

LC parallel resonance is composed of VC1, VL1, C25, in parallel with C26, C27 C28 and C24. The bandwidth is selected by the PIN diodes (CR2 and CR4) switching. When one of the RBW Filters in LC Mode selected, the corresponding control line is +14 Vdc, and the others not selected are –14 Vdc. The highest resistance of R21 and R26 results in narrowest bandwidth (30kHz). On the contrary, the lower resistance results in the widest bandwidth (3MHz). The loss of the LC filter bandwidth is compensated by the feedback through Rfb.

(4) Crystal Filters (1st, 2nd, 3rd, 4th and 5th)

Y1 is the equivalent circuit of the crystal filter. This circuit block functions in the series resonance mode but Co and Rs are undesired. The circuit is compensated as follows: The current (-I1) through Q4, C38, VC2 and the current (I1) through Co of the Y1 cancel each other. Rs, is canceled as follows: The positive feedback of Q3 will generate (-Rs), which cancels Rs. R40, C41, VC3, and L10 provide parallel resonance to compensate unwanted capacitance, which are the input capacitance of the buffer amplifier, PCB capacitance, and PIN diode (CR8) capacitance. PIN diode (CR8), will apply a variable resistance adjusted by current. The series resistance determines the bandwidth in this series resonant circuit.

The DC bias voltage is +9V, and the resistance of CR8 is dependent on the BWXT line voltage. The more current that flows through CR8, the smaller the resistance will be. Thus, higher Q is formed and the passband is narrower. On the contrary, current that flows through CR8, the larger the resistance is. Thus, lower Q is formed and passband is wider.

STEP-GAIN AMPLIFIER (-15.9 to +50.0dB)

(1) Amplifier (0/10dB)

This circuit is configured as a non-inverting op amp. It has 2 functions: one is to switch +10dB gain on/off and the other is to adjust the IF offset gain to approximately +12dB. Gain is adjusted by VR6 and switched by the bias state of CR30. In the forward bias condition of CR30, +10dB line goes to about 0.20Vdc, and the amp has +10dB Gain. In the reverse condition, this about 14 Vdc, the amp functions as a voltage buffer.

(2) Amplifier (0/20dB-1,2,)

This circuit is similar to the above Amplifier circuit except with +20dB. Gain is adjusted by VR4 (VR5) and switched by the bias state of CR28 (CR29). In the forward condition of CR28 (CR29), +20dB line goes to about 0.20Vdc, and the amp has +20dB gain. In the reverse condition, this about 14 Vdc and the amp functions as a voltage buffer.

(3) Step-Attenuator

The step Attenuator provides the following attenuation values:
0.1dB, 0.2dB, 0.4dB, 0.8dB, 1.0dB, 2.0dB, 4.0dB, 8.0 dB
These are respectively switched to 'on' or 'off' states for setting desired IF Gain. Each stage contains the same circuit, and the attenuation value is dependent on the ratio of Ra and Rb. In the forward bias condition of CRa, -x.xdB line goes to about 0.16Vdc, and it has x.xdB attenuation. In the reverse bias condition, the voltage is about 14 Vdc and the amp functions as a voltage buffer.

IF OUTPUT(ⓔ)

(1) Out Driver

One output is connected to the VIDEO DETECTOR - Board(A4), the other output is connected REAR PANEL.

(2) IN/Out Gain Change

In the RBW300, RBW (300-G) line goes to about 0.2 Vdc. The input gain is about 3.75 dB and output gain is about 10 dB. In the other RBW selections, CR7a and CR58 are reverse biased. The input gain is about 10.67 dB and the output gain is about 0 dB. Also, in the RBW300 mode, IF Board Offset Gain includes about 3 dB for the compensation of it's higher loss.

Video Detector Board Assembly

General

The input signal is received and down-converted in the RF module, amplified and filtered in the IF module and then applied to the Video Detector module. The desired information of the signal (e.g. LOG/LINEAR, FM/AM, QP) is detected in the video detector stage, then the signal is converted into a DC voltage signal which can be digitally processed. The video detector stage will perform one of the following:

- The amplitude of the input signal can be converted into log scale (in the log detector circuit)
- The amplitude of the input signal can be converted into linear scale (in the linear detector circuit)
- Modulation signal processing: AM/FM demodulation
- Trigger signal processing: reference level adjustment when processing the signal (for Video, Line, Ext, and GND)
- Quasi peak (option): EMC measurement function (Band B or C available)

Log Detector

A 10.7 MHz signal received in the video detector board passes through the 5MHz band pass filter, and fed to the Logarithmic Amplifier IC (U3), when operating in the LOG display mode. The bandwidth of the 5MHz Band pass filter is wider than that of the maximum RBW filter of the IF AMP board. The 5MHz Band pass filter reduces the noise of the signal that is fed to the Logarithmic Amplifier IC (U3). The output range is changed by adjusting slope (gain) and offset in the circuit after the Logarithmic Amplifier IC (U3). Use VR2 for slope adjustment and VR1 for Offset adjustment. The adjusted signal (-366mV to + 366mV) is sent to the Video select IC (U20) through the switch IC (U10) and the Video buffer amplifier.

Linear Detector

A 10.7 MHz signal received in the video detector board passes through the linear detector circuit when operating in the LIN display mode. The input signal is applied to a Balun (transformer) splitter, to provide two sources. One passes through the preamplifier, limiter amplifier, and the filter. Then, it is applied to the mixer LO input port. The other passes through the Amplifier and the filter, and it is applied to the mixer RF input port. The RF signal and the LO signal are applied to a double-balanced-mixer. The IF output signal of the mixer passes through the Duplexer, then the signal is converted into a DC signal. The duplexer is composed of a 8MHz Low pass filter and a 8MHz High pass filter. It reduces intermodulation products, and improves linearity of the output IF signal. Gain adjustment (VR3) and Offset adjustment (VR10) are performed on of the signal converted into DC for the purpose of signal processing in the Processor Boards A to D converter. The adjusted signal (-366mV to 0mV) is sent to the Video select IC (U20) through the switch IC (U10) and the Video buffer.

AM/FM Demodulator

A 10.7 MHz signal received in the video detector board passes through the buffer Amplifier, attenuator to obtain the desired level, DC block capacitor for DC signal rejection, and automatic gain control (AGC) circuit. The signal is amplified 20dB in the amplifier before passing through the 10.7 MHz tuning transformer, and is sent to the AM/FM detector at the appropriate level. The AM signal is demodulated while passing through the schottky diode. Demodulated Audio (or Video information) is adjusted to an appropriate size in the audio buffer and the amp, then it is sent to the Video select IC (U20).

Temperature Sensor

The temperature sensor uses diode temperature variation factors to provide a voltage proportional to temperature. It senses the internal temperature of the analyzer. The internal temperature is used as data and is needed to perform temperature calibration.

Quasi Peak Detector (Option)

The quasi peak detector uses a linear detected video signal. The charge time constant and the discharge time constant of this signal is set by the peak detector RC circuit according to the bandwidth. The mechanical time constant is supplied from the low pass filter. This signal is sent to the video select IC (U20).

Video Source Selection

Seven video circuits are connected to video source select. The switch IC (U20) performs video selection. The follow is a list of connections to the video selection IC (U20):

- The quasi-peak signal is connected to the quasi-peak detector circuit. (option)
- The LOG/LIN signal is connected to the LOG/LIN detector circuit. (LOG/LIN display mode)
- The temp sensor signal is connected to the temp sensor circuit. (This is only during temperature calibration operation)
- The FM signal is connected to the FM modulation circuit. (FM display mode)
- The AM signal is connected to the AM Demodulation circuit.
- The FILT-TE signal is connected to the SGTE-CH connector on the rear panel. Use it after inserting the jumper pin to test the video filter on the video detector board.

Video Filter

The signal selected in the video source passes through the video low pass filter. The video filters are:
10Hz, 30Hz, 100Hz, 300Hz, 1kHz, 3kHz, 10kHz, 30kHz, 100kHz, 300kHz, 1MHz and None
The bandwidth cutoff frequency is selected by changing resistor and capacitor values (by selecting switch IC). Cutoff frequency range are defined as the point at which 70.7% of the input signal is present at the output.

Trigger

Trigger source select is connected to three trigger sources as follows:

- The line trigger signal is sent from the power supply through the AC line (sine wave, > 1 Vp-p, 60Hz)
- The External Trigger signal is sent from the external input connector on the rear panel. (10 Vp-p)
- The internal video signal is sent from the video filter output.

The signal selected among the above three signals by the IC switch passes through either a 100kHz low pass filter or a 5Hz high pass filter, then it reaches the voltage comparator. The comparator sends the output by comparing with the trigger levels. (-400 mV to +400 mV) The trigger signal level and the squelch signal level, are set by the DAC IC. (U34)

Processor Board Assembly

Processor board assembly receives keyboard-inputs, controls the system, processes the signal inputted from the video detector assembly, and displays it on the LCD screen. The roles of the main parts are as follows:

Central Processing Unit

The main CPU is an Intel 386EX embedded micro controller. It is embedded with several peripherals, such as an address bus of a 32-bit data bus internally, but a 16-bit external data bus. It also has a chip-select unit, a clock & power management unit, a DRAM refresh control unit, an I/O port, an interrupt control unit, a timer/counter unit, and an asynchronous serial an I/O with 2 channels. It performs main control as well as computation, and the peripheral graphic controls, RS-232C or printer.

Digital Signal Processor

A Digital Signal Processor (ADSP 2171) is used as a secondary processor. This processor is a 16-bit fixed point DSP. It is embedded with a HIP (Host Interface Port), 2k words of program memory, and 2k words of data memory. Real-time over-sampling and synthesizer control, are provided as well as digitizing.

Bus Controller

The bus controller (Radisys R300EX) generates three main memory signals, a DRAM address signal, a control signal, and an ISA bus control signal.

LCD Controller

A logic cell array (Xilinx XCS10-3) is used for the LCD controller. Separate VGA BIOS is not needed. The VLINE function is implemented with H/W. Video signals are sent to the screen at high speed. The controller receives graphic data from the main CPU, controls the video memory, and sends screen data output to the LCD module. A DC-DC converter (MAX749) is used to control the LCD contrast. It generates about -17V to control the LCD contrast.

I/O Controller

A logic cell array (Xilinx XCS10-3) is used for the I/O controller. The controller decodes the main CPU I/O address, and generates control signals in the IF filter & AMP, Video Board. It interfaces with the keyboard and implements frequency counter functions.

Synthesizer Controller

A logic cell array (Xilinx XC5202-6) is used for the synthesizer controller. The controller decodes the address of the secondary processor. It generates control signals in the synthesizer board, ADC control, and the IC timer and sweep time control signals.

GPIB Controller

A NAT9914 is used for the GPIB controller. This controls the GPIB port. It is connected to the GPIB connector on the rear panel using bus transceiver 75160 and 75162.

Data Buffers

Two units of 16 bit data buffer (74ABT16245) are used for the data buffer. The data buffer provides buffering for the main CPU and secondary processor ISA bus.

Analog to Digital Conversion

A 12-bit analog to digital converter (LTC1272-3) is used for ADC. The ADC digitizes the video signal from the Video module.

Battery Backup

The SRAM power supply is used for SRAM battery backup when the power is off.

Memory

There are four types of memory. PA28F400 is a 4M-bit flash memory. Programs are stored in it. GM71C18160 is a 16M-bit memory. Data is stored in it when the program is executed. KM6161000 is a 1M-bit SRAM. This is used in conjunction with the backup battery. The user setup data, graphic data and calibration data are stored in it. GM71C4260 is a 4M-bit DRAM. This is used for video memory.

Main signal flow is as follows (see the Processor Block Diagram):

(1) Video Signal

The Video signal is fed from the video board, is digitized in the ADC, is compressed and processed for the proper detection mode in the secondary processor (DSP), is output to the main CPU, computed using calibration data, and output to the LCD module through the LCD controller.

(2) Interrupts

The key scan input signal of the I/O controller generates a key interrupt signal. The main CPU reads this signal and processes it. The control signal in each module generates signals in the I/O controller (receiver, IF filter & AMP, and video detector control signal), DSP, and synthesizer controller and controls each module.

(3) Peripherals

The RS-232C and printer port (external interface signals) control is connected to the rear panel through the I/O port of the main CPU. GPIB circuiting is connected to the rear panel through the GPIB controller and the bus transceiver. PCMCIA (option) is connected to the PCMCIA slot through the 164-pin connector and the motherboard.

Motherboard Assembly

The motherboard assembly is the interconnect of the system, connecting each module and assembly to the power supply and the system processor assembly. The motherboard assembly allows transfer of data and control signals needed for each part of the spectrum analyzer system. Control signals of the RF module, IF AMP board, video detector board, and Tracking Generator (option) are transferred/received through the motherboard from the FPGA (U23, U14) of the system processor board.

P61 (96-pin): RF module

The RF block assembly is composed of the receiver board (7010-2530-600) and the synthesized board (7010-2630-500) which are connected to the motherboard by P61. Data and control signals are passed to and from the RF module. Supply voltages used are +24V, -15V, +15V, and +5V.

P62 (96-pin): Tracking Generator Board (option)

Tracking Generator is composed of the tracking generator control board (511-645-A) and the tracking generator RF board (511-653-A). It is connected to P62 of the motherboard. Data and control signals are passed to and from the module. Supply voltages used are -15V, +15V, and +5V.

P63 (96-pin): IF filter Board

The IF Filter Board (511-649-A) is connected to P63. Data and control Signals are passed to and from the module. Supply voltages used are -15V, +15V, and +5V.

P64 (96-pin): Video detector Board

The Video Detector Board (511-648-A) is connect to P64. Data and control signals are passed to and from the module. Supply voltages used are -15V, +15V, and +5V.

P65 (96-pin), P66 (64-pin): Processor Board

The System Processor Board (511-646-A) is connected to P65 and P66. Data and control signals are passed to and from the module. P66 is connected to the PCMCIA board. Data bus, ADDR bus, and control signals are provided through P65. Supply voltages used are -15V, +15V, +12V and +5V.

P67 (80-pin): PCMCIA Board (option)

The optional PCMCIA Board (511-650-A) is connected to P67. It provides P66 with Data bus, ADDR bus, and control signals.

P68 (44-pin): Power Supply Module

Supply voltages (+24V, +12V, -15V, +15V, and +15V) generated in the power supply module is provided to each connector and wire harness of the motherboard. Supply voltages –15V, +15, and +5V pass through the EMI filter FL1 (+5V), FL2 (+15V), and FL3 (-15V) in order to minimize ambient noise in the system.

Miscellaneous

The **Cooling Fan** (639-010-A) is connected to P612 (3-pin) and is provided with (+12V) from the power supply.

The **Audio Speaker** (637-021-A) is connected to P614 (2-pin) and audio information is provided from the system processor board.

The **LCD Inverter Assembly** (511-647-A) and RF Input Protection Assembly (511-658-A) are connected to P616 (4-pin). P616 provides the LCD inverter Assembly with (+12V) and the RF input protection Assembly with (+15V and –15V) from the power supply.

The **Medium Stability Oscillator** (511-660-A) or optional **High Stability Oscillator** (7010-263-0700) time bases ae connected to P617 (3-pin). P618 provides the time base assemblies with (+15V) from the power supply as well as the control signal (INT_EXT) from the system processor assembly.

The **10 MHz Reference In/Out** is connected to P618 (2-pin). The 10 MHz Reference In/Out is route through the wire harness and then to the rear panel BNC connector.

LCD Inverter Assembly

The LCD Inverter Assembly is the circuitry necessary to invert low voltage DC to high voltage AC. This high voltage is to provide power to the backlight in the LCD assembly. The power supply provides DC (+12V ±2%) to the LCD inverter assembly through the motherboard and the wire harness (550-922-A) and converts this to high voltage AC (1000~1500Vrms). **Use extreme caution when testing and troubleshooting this high voltage inverter assembly.**

Keyboard Assembly

The Keyboard Assembly consists of the Standby/Power-On switch and all switches that are used the control the functions of the 2398. The keyboard assembly is a matrix of switches that provide row and column information when a key is pressed. This information is then transferred through the wire harness (550-914-A) to the system processor assembly (511-646-A) to control the analyzers functions.

Power Control and Indication

There are two LED indicators (yellow and green), located on the front panel next to the Standby/Power-On key. These indicators represent the condition of the analyzer, yellow for Standby and green for Power On. A short press on the Standby/Power-On key will turn on the analyzer, however it is necessary to press and hold the Standby/Power-On key for about 5 seconds in order to power down the analyzer.

Function, Control, Data Entry Step Keys and the Scroll Knob

The analyzer functions are control by pressing these keys When a key is pressed, row and column information is sent to system processor assembly through the wire harness (550-914-A).

AC Power supply Assembly

This consists of AC input, EMI filter, rectifier circuit, PWM control, switching trans, feedback, secondary rectifier, and output.

INPUT: 90VAC -264VAC

EMI Filter

The EMI filter removes the electromagnetic wave generated by the Switching Power Supply. C1 and L1 remove the low bandwidth from the electromagnetic wave, C2 and L2 remove intermediate bandwidths of the electromagnetic wave, and C3, 4, 15 and 23 remove high bandwidths of the electromagnetic wave.

Rectifier Circuit

The Rectifier Circuit converts the INPUT AC voltage into DC voltage. Ripple voltage is generated when the INPUT voltage passes through BD1. DC voltage comes out when the ripple voltage flows into C6, C6-1.

PWM Control

The PWM Control (KA 7552) is applied to PWM CONTROL IC. When voltage is applied to the VCC (PIN6) of the U1 (KA7552) through R2, basic operation of U1 begins. When voltage is applied to the VCC of U1, a square-wave will be on PIN5 at the frequency selected using RT and CT. This waveform is supplied to the gate of Q1 through R5, R40. When Q1 begins operating, the drain of Q1 conducts electricity and Q1 is turned on and off. Voltage is quickly transferred to PIN14,16 of T1 by the Q1 operation. Switching voltage is generated according to the winding ratio of the first, the secondary and AUX parts of T1. AC voltage is sent to the secondary and AUX(power supply terminal of U1) parts. Voltage sent to PIN12 of T1 passes through R45 and CR2. Then, VCC voltage is supplied to U1. R45 is the VCC guard voltage of U1. It suppresses peak voltage when turning on the power. CR4 in U1 output is a 'speed up' diode. It quickly removes residual current when turning off the gate of Q1.

Secondary Rectifier

The Secondary Rectifier converts the voltage sent to T1 into DC voltage using the electrolytic condenser in CR8, CR9, CR10, CR11, CR12 and in each terminal.

Feedback

Feed Back is caused by +15Vdc of output. The secondary rectified voltage is fed back by U3 and U7. Current flows into PIN1(LED ANODE) of U3 through R15. Then the LED is illuminated. The amount of illumination can be adjusted using U7. U7 is a programmable IC. The internal reference voltage is 2.5V. In the case that the reference voltage (PIN3) is 2.5V or higher, current flows from the cathode to the anode. In the case that the reference voltage is below 2.5V, current is less intense. Current flows from PIN4(collector) to PIN3(emitter), and the current adjusts FEED BACK CONTROL of PIN2 of

U1. Voltage change of FEED BACK(PIN2) controls the pulse width of output(PIN5) so the on/off time of Q1 can be controlled. As switching on/off time of T1 is adjusted, the quantity of secondary switching of the AC voltage is adjusted. E.g, the voltage sent to the secondary part is higher than the reference voltage (+15V or higher)

When more current than the reference flows into R20, the reference voltage of U7 increases, so intense current flows from the cathode of U7 to the anode. Then, the quantity of current which flows from PIN1(anode) of U3 to PIN2(cathode) increases, and the amount of illumination of the LED increases. When the base of the photo TR in the first rectifier part receives the light, current flows from PIN4(collector) to PIN3(emitter) and the voltage of PIN2 of U1 will decrease. Then, the output(PIN5) pulse width of U1 decreases. The switched voltage sent to the secondary part through T1 decreases according to the ON time change of Q1. In the case of the output voltage being below the reference voltage, the voltage sent to the secondary part increases. The output voltage is maintained in a fixed state due to repetition of this operation.

5v Standby Power

5Vdc Standby Power is supplied from Smart IC (1M0280). The existing IC is separately designed for PWM and FET. Smart IC needs only one design for both.The VCC, auxiliary power, feed back and surrounding circuits became very simple. The frequency is now fixed (to 50 kHz). The U17 of the smart IC starts operation when the current flows into PIN3 of U17 through R28. Then, PIN2 of U17 starts converting, and the converted voltage is generated in T2 and the converted AC voltage is sent to the second part. The, rest of the operations are the same as the principles of main circuit operations

Line Trigger

Line Triggering is possible due to U6. U6 turns on/off input AC voltage and the LED (60Hz) of U6 through R13and R14. Then the base of the photo TR of U6 is driven, and a square-wave is outputted in a 60Hz cycle.

PCMCIA Card Slot Assembly (Option)

The PCMCIA Card Slot Assembly is the circuitry necessary to interface with a PCMCIA Type 1 SRAM Memory Card. This optional assembly allows the analyzer to read and write such information as analyzer setup information, waveform data, and images (BMP) from the processor board.

Tracking Generator Module Assembly(option)

Overview

The Tracking Generator is the RF Signal Source. The output frequency, which can be set or swept by TG1LO (3410.7~6110.7MHz), can come out within the range from 100kHz to 2.7GHz. The output power, which can be controlled by the setting of 10dB Step Attenuator and Level DAC, is within the range from 0dBm to -70dBm. Its output frequency equals the subtraction of 3410.7MHz from the TG1LO. By Providing LO signal the same that LO of Spectrum Analyzer for LO port of the Tracking Generator, the frequency of TG OUT is synchronized with the received frequency of Spectrum Analyzer. Largely divided in the respect of function, Tracking Generator has 2 blocks. One is ALC(Automatic Level Control) which stabilizes the level of TG OUT, the other is PLL(Phase Locked Loop) which does the frequency of TG OUT.

ALC (Automatic Level Control)

1) General description of ALC

A 3410.7 MHz signal is generated in the DRO (Dielectric Resonant Oscillator) block and coupled to VGA (Variable Gain Amplifier) block by the DC (directional coupler). The input power level of the VGA is about –13 dBm, which is determined by the coupling coefficient of the DC and the DRO output power. The controlled voltage (VGA CTRL) adjusts the gain of the VGA and its level is determined by the output of the Detector and Level DAC. The Detector discriminates the quantity of output power, and converts voltage proportioned to it, while the Level DAC sets the reference voltage proportioned to desired output power. The detected voltage is differentially amplified, added, amplified, and sent to the Loop Filter, which compares the reference voltage at a specified output power level with the detected voltage, amplifies, and filters it. The TG output frequency is determined by the frequency of the LO. The 3410.7MHz (VGA Output Frequency) and LO frequency are mixed with each other. This mixed output frequency (IF) is filtered by LPF1, amplified by 2 stages of 20dB Amps, and attenuated by the 3dB Attenuator at the input and output of th 20 dB Amp. This amplified output is sent to the Detector directly and to the TG OUT, passing through the 3dB Attenuator and 10dB Step Attenuator.

2) VGA (Variable Gain Amplifier)

The VGA is composed of two amplifiers and two PIN π attenuators. This block has about 30 dB fixed gain and variable attenuation, which is controlled by the voltage (VGA CTRL). The voltage (VGA CTRL) sets the DC bias current of the PIN diode, which, subsequently determines the amount of attenuation of the PIN π attenuators.

3) Mixer

The Mixer has two inputs (LO & RF) and one output (IF). The RF signal (3410.7MHz) comes from the DRO and the LO signal (3410.7 to 6110.7MHz) comes from the TG1LO. The frequency of the IF depends on that of the LO as the RF signal frequency is constant and the LO signal frequency is variable. TG1LO is amplified sufficiently enough to drive LO of the Mixer by the LO AMP. The

Mixer is composed of a Schottky diode, Microstrip Coplanar waveguide, and a Microstrip Slotline. To satisfy wideband characteristic at the LO port, a Balun is designed taking advantage of the Coplanar waveguide. This LO signal is arrived at the Schottky diode by the transition from the Coplanar waveguide to the Slot line. The RF and IF signals are separated by the Microstrip T-Junction. The frequency of TG OUT is the same as the IF output.

4) Detector and Amplifiers

The main role of this block is to detect the RF power level. Positive and negative signals detected are respectively amplified 4 times, and added.

5) Loop Filter and Level DAC

The power level of TG OUT is determined according to respectively established DAC Code, of which the range exist from 0.0dBm to –9.9dBm and the resolution is 0.1dB. This Code is reference voltage to be compared with the detected voltage. The difference of them is amplified, filtered, and result in voltage (VGA CTRL).

PLL(Phase Locked Loop)

1) General description of PLL

3410.7[MHz] is oscillated in the DRO Block. DR is the initial of the dielectric resonator, used main component of the DR Oscillator. The output frequency of the DDS (direct digital synthesizer) can be set and adjusted by 32bit digital binary code. For the purpose of making

2) VTO (Voltage Tuned Oscillator)

TR has potentially of being unstable by using series feedback, and the DRO (Dielectric Resonator) is magnetically coupled with microstripline, which is connected to input of the amplifier. The lengths of microstriplines connected base and emitter are designed to satisfy the condition that can be oscillate. The output of TR, namely collector, has matched microstripline circuit to make maximum output power. The DRO is magnetically coupled with microstripline and varactor. As the voltage(DRO_CTRL) of varactor changes, the capacitance of it does, and consequently output frequency of DRO does. Also, to adjust the frequency manually, the cover of DRO has tuning screw of which the height determines it.

3) SPD (Sampling Phase Detector)

High frequency signal having high stability and low noise generally can be acquired from the harmonics of stable low frequency like Crystal Oscillator. SPD block has 2 functions. One is frequency multiplier, which makes 43 times of the 80MHz. For this application, a SRD (Step Recovery Diode) is used. It has very high capacity on the state of positive bias, has small on the state of reverse, and can be thought as high efficient switch controlled by the electric charge. Having very short transition time (about a number of pico sec), it can generate acute impulse to have very high efficiency at high order harmonics. The other is frequency mixer, which mixes 3440MHz (43×80MHz) with 3410.7MHz (the frequency of DRO) and yields the different frequency between them. In front of the SPD block, there is a Balun Transformer to sustain 180 phase difference at single balanced mixer. The output frequency of the SPD passes Bandpass Filter, and is amplified with about 54[dB] gain at 29.3MHz. The other IF frequency, 50.7MHz, should be sufficiently suppressed. To accomplish this end, the IF(29.3M) passes through the Bandpass Filter to have about 30[dB] attenuation at 50.7MHz.

4) DDS (Direct Digital Synthesizer)

A frequency output is controlled by 32-bits binary code, and its dada is determined by this equation;

$$(Fout/80M) \times 2^{32}.$$

Except the frequency of DDS output, many other frequencies come out like this;

Fin-Fout, Fin+Fout, 2Fin-Fout, 2Fin+Fout, 3Fin-Fout, 3Fin+Fout.

The level of these frequencies is about -3~ -10[dBc]. But, it was designed to suppressed fully by the placing of 5-pole elliptical LPF which is recommended on the selected DDS Datasheet.

121-809-A

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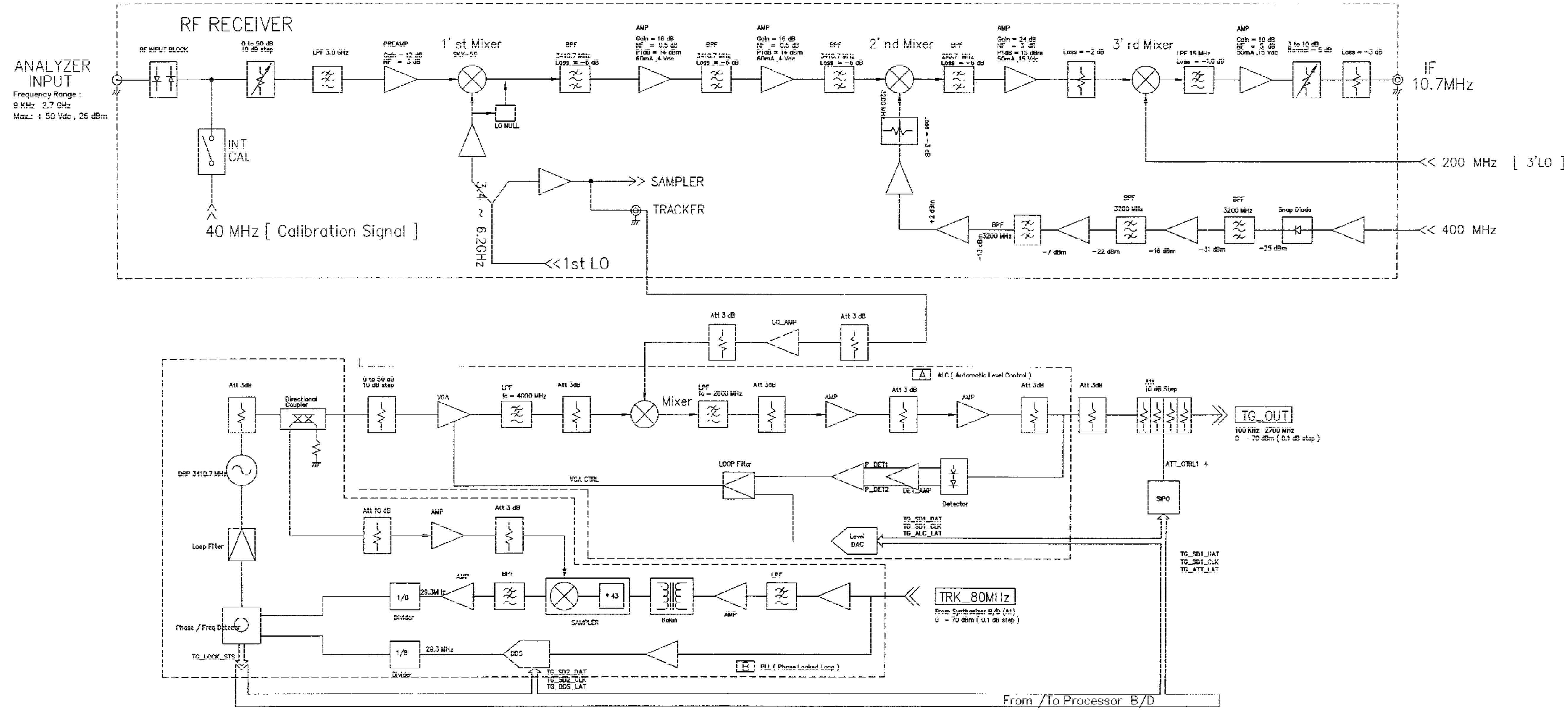

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121-809-A

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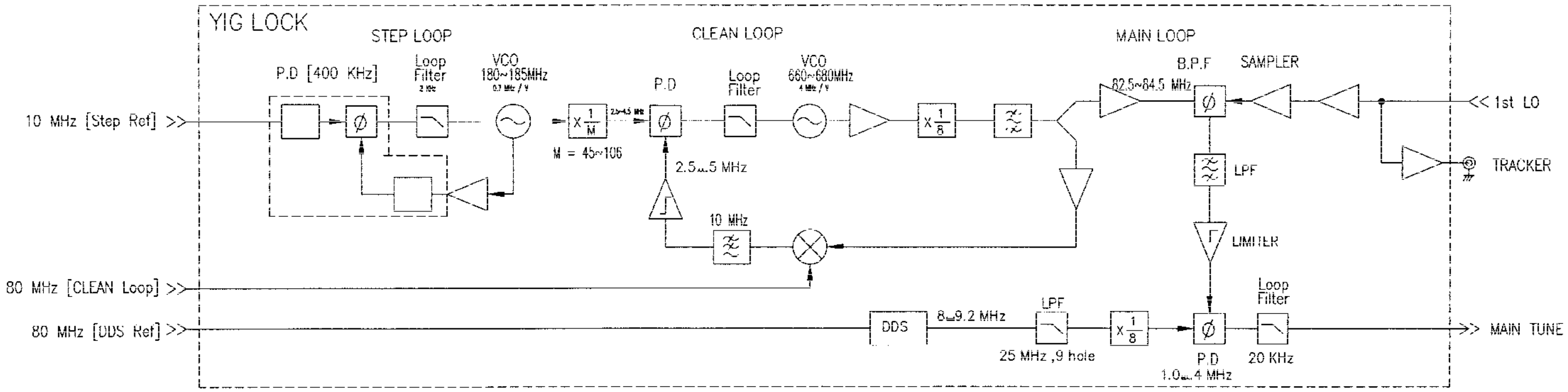

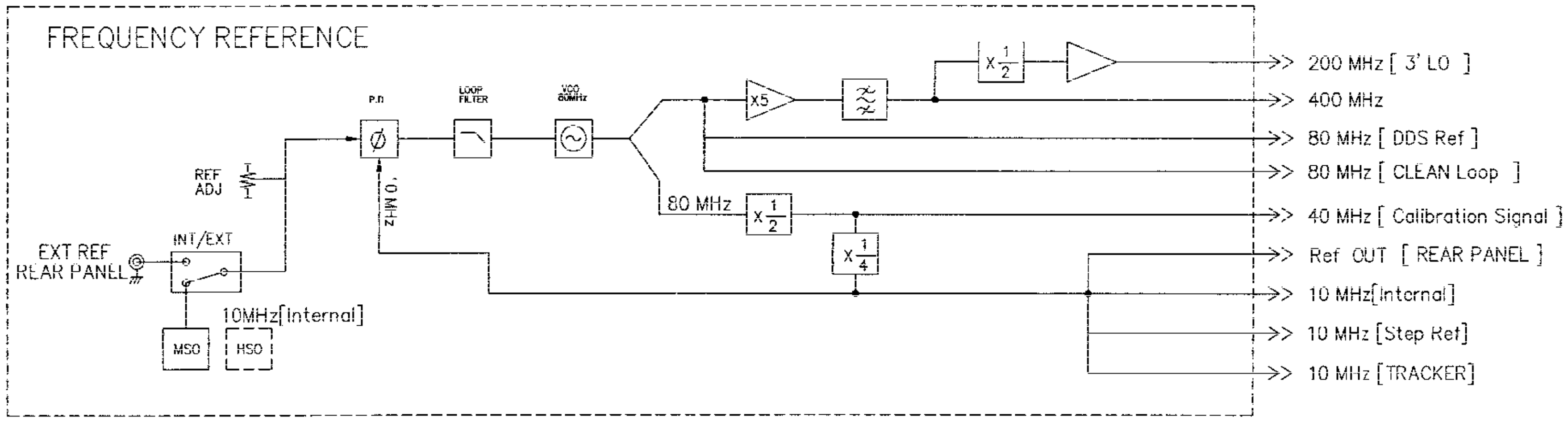

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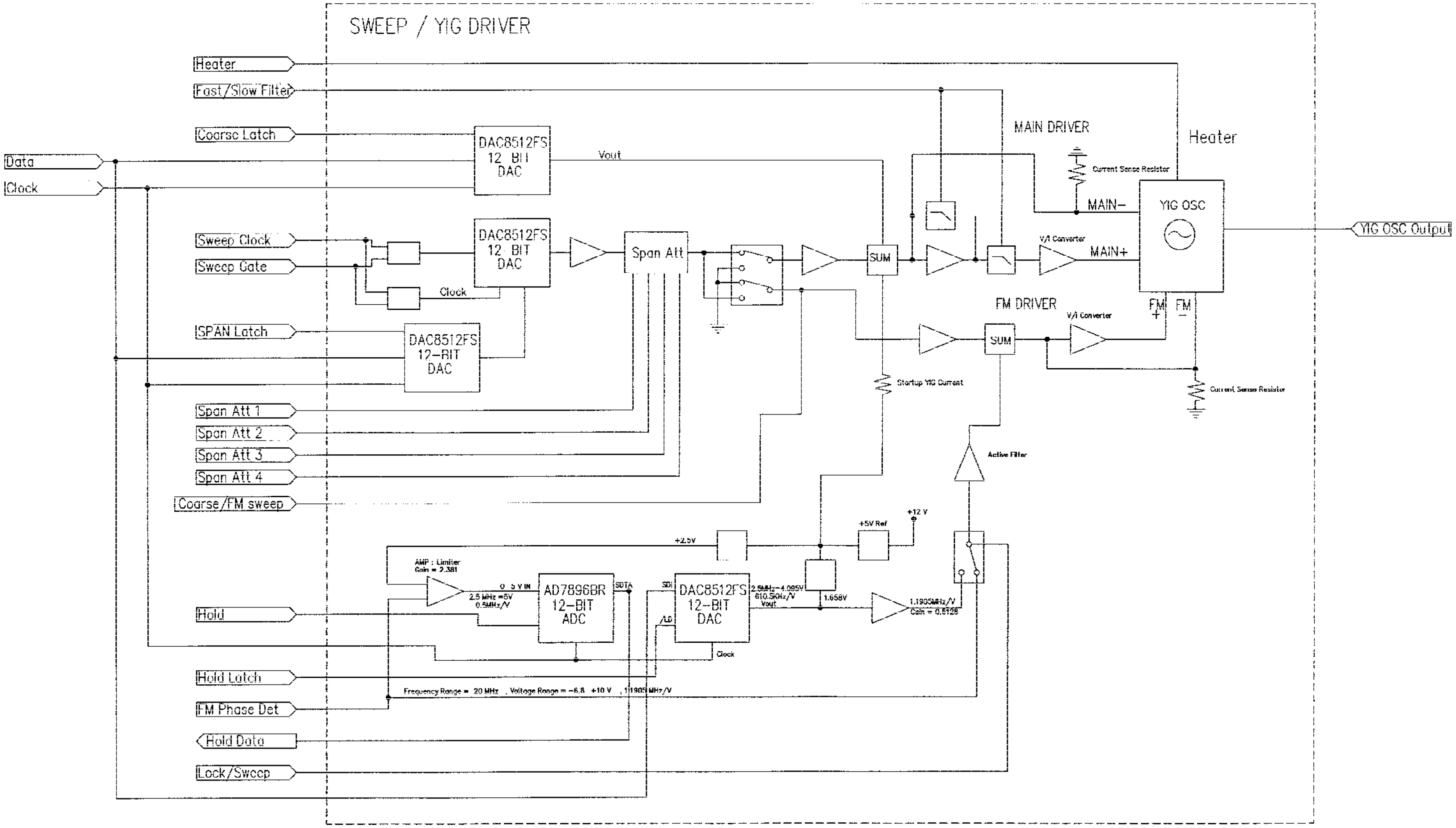

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121-809-A

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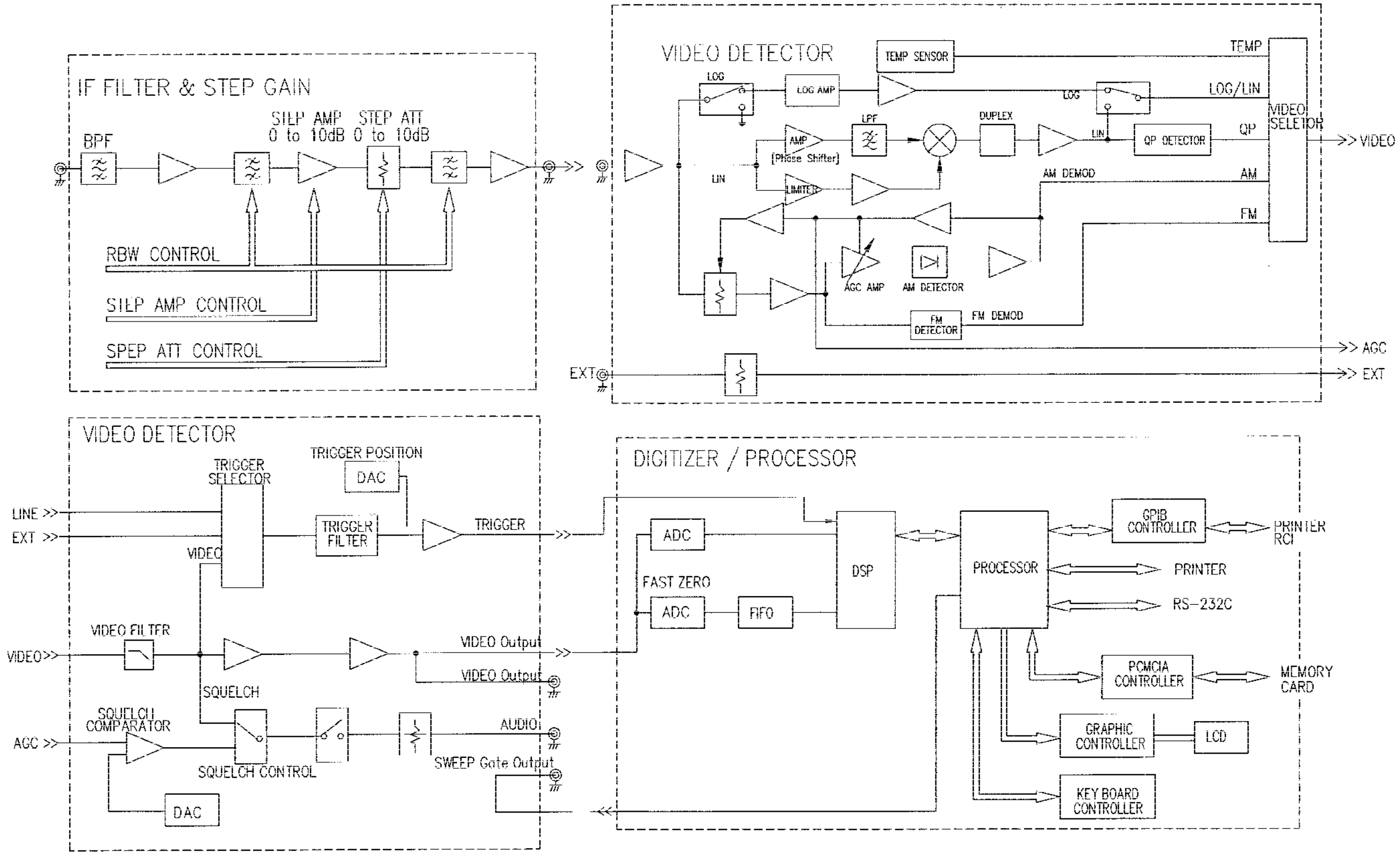

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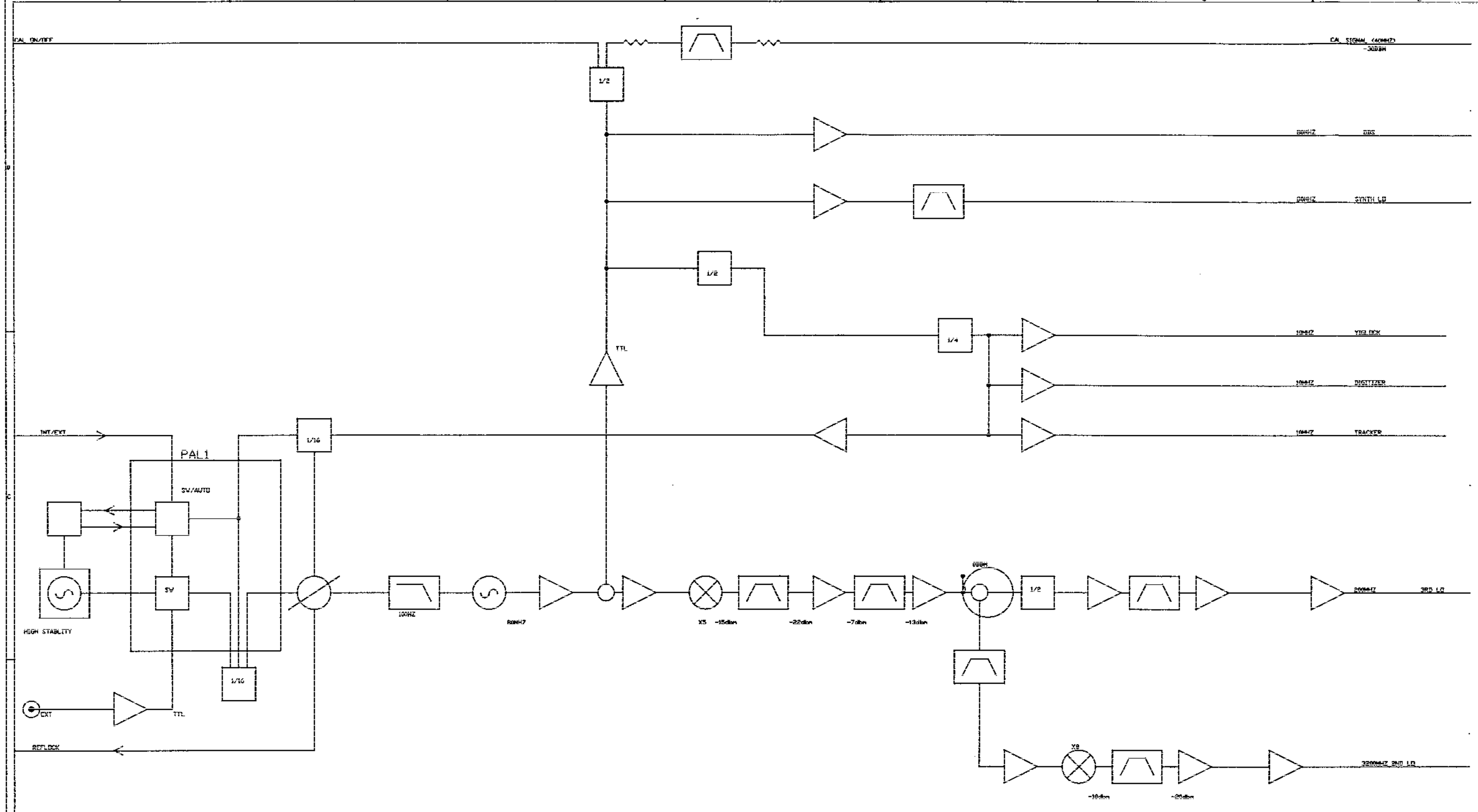

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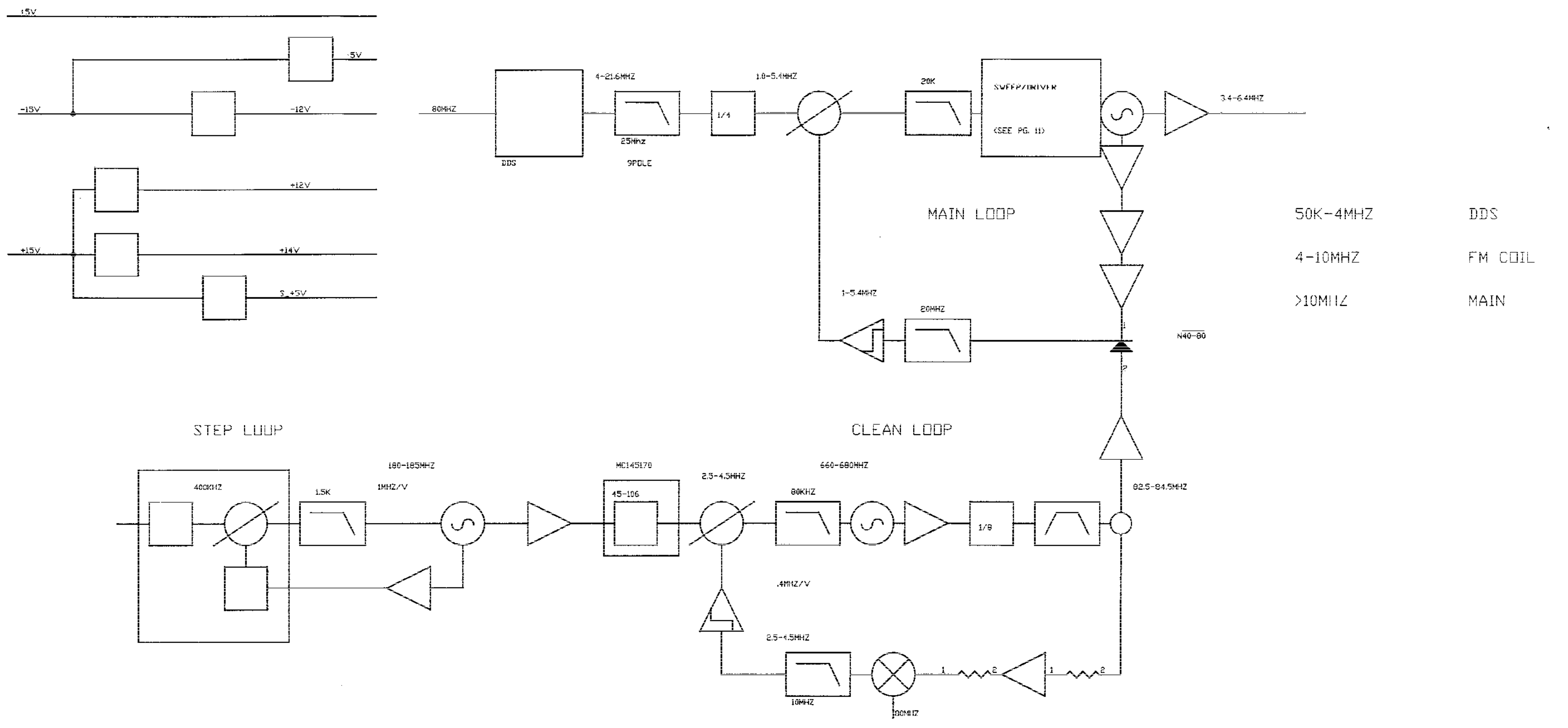
Size C	Document Number 7010-2630-500	REV F0
Date: February 12, 1999	Sheet 9 of 11	



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Date: February 12, 1999	Sheet 10 of 11	

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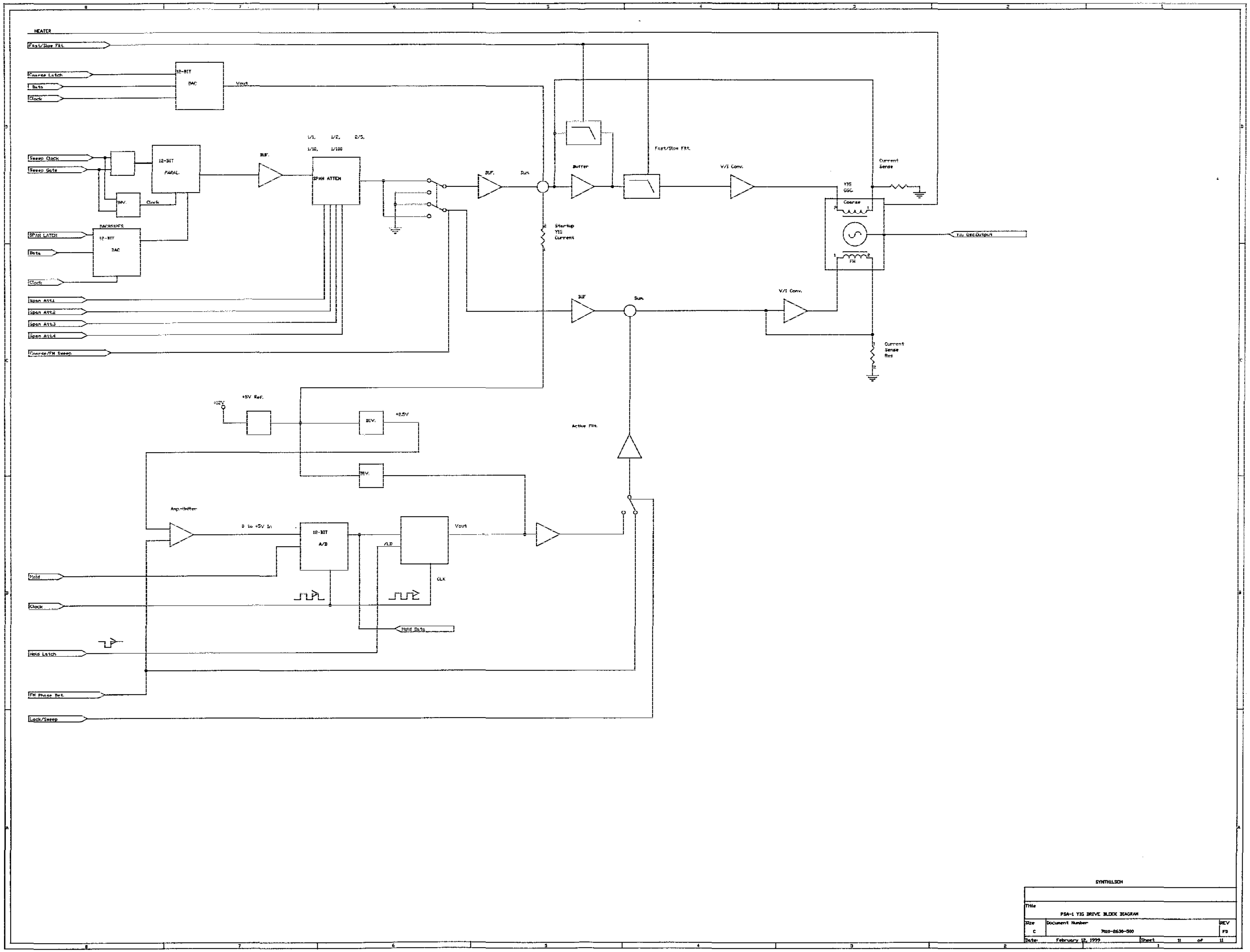
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Coarse Latch
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12-BIT
DAC
Vout
Sweep Clock
Sweep Gate
12-BIT
PARAL.
Clock
SPAN LATCH
12-BIT
DAC
Data
Clock
Span Att1
Span Att2
Span Att3
Span Att4
Coarse/FM Sweep
BUF.
1/1,
1/2,
2/5,
1/10,
1/100
SPAN ATTEN
BUF.
Sum
Buffer
Fast/Slow Filt.
V/I Conv.
Current
Sense
YIG
OSC.
Coarse
FM
YIG OSC Output
Startup
YIG
Current
BUF
Sum
V/I Conv.
Current
Sense
Res
+12V
+5V Ref.
DIV.
+2.5V
DIV.
Active Filt.
Amp-limiter
0 to +5V In
12-BIT
A/D
/LD
Vout
CLK
Hold
Clock
Hold Data
Hold Latch
FM Phase Det.
Lock/Sweep
SYNTHILSCH
Title
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Size
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REV
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Date
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11
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11

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511-649-A

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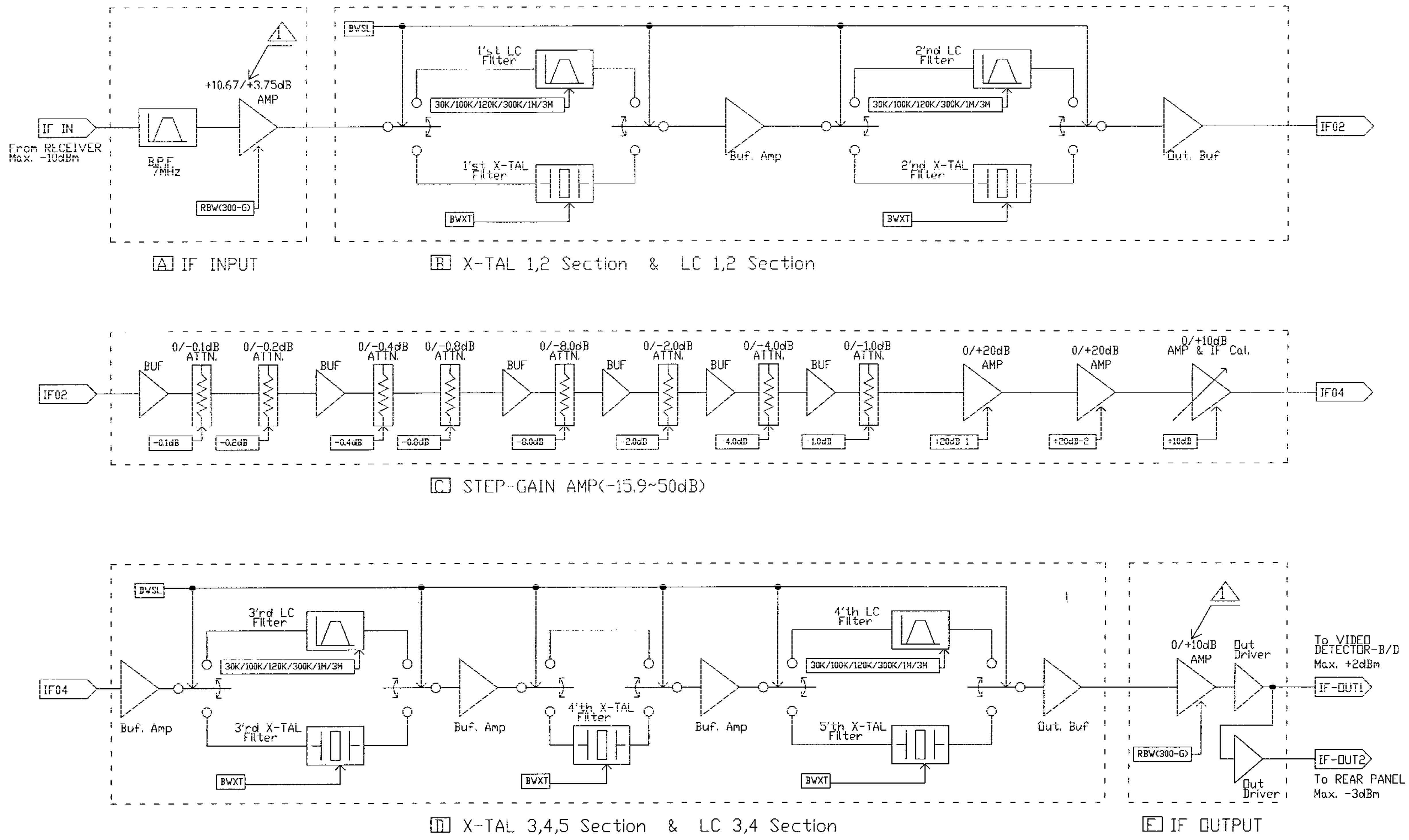

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DESIGNED
CHECKED
VERIFIED
APPROVED

TITLE IF FILTER-B/D (A3)

SIZE A4 | DWG. NO 511-649-A

SCALE | UNIT | SHEET 8 OF 8

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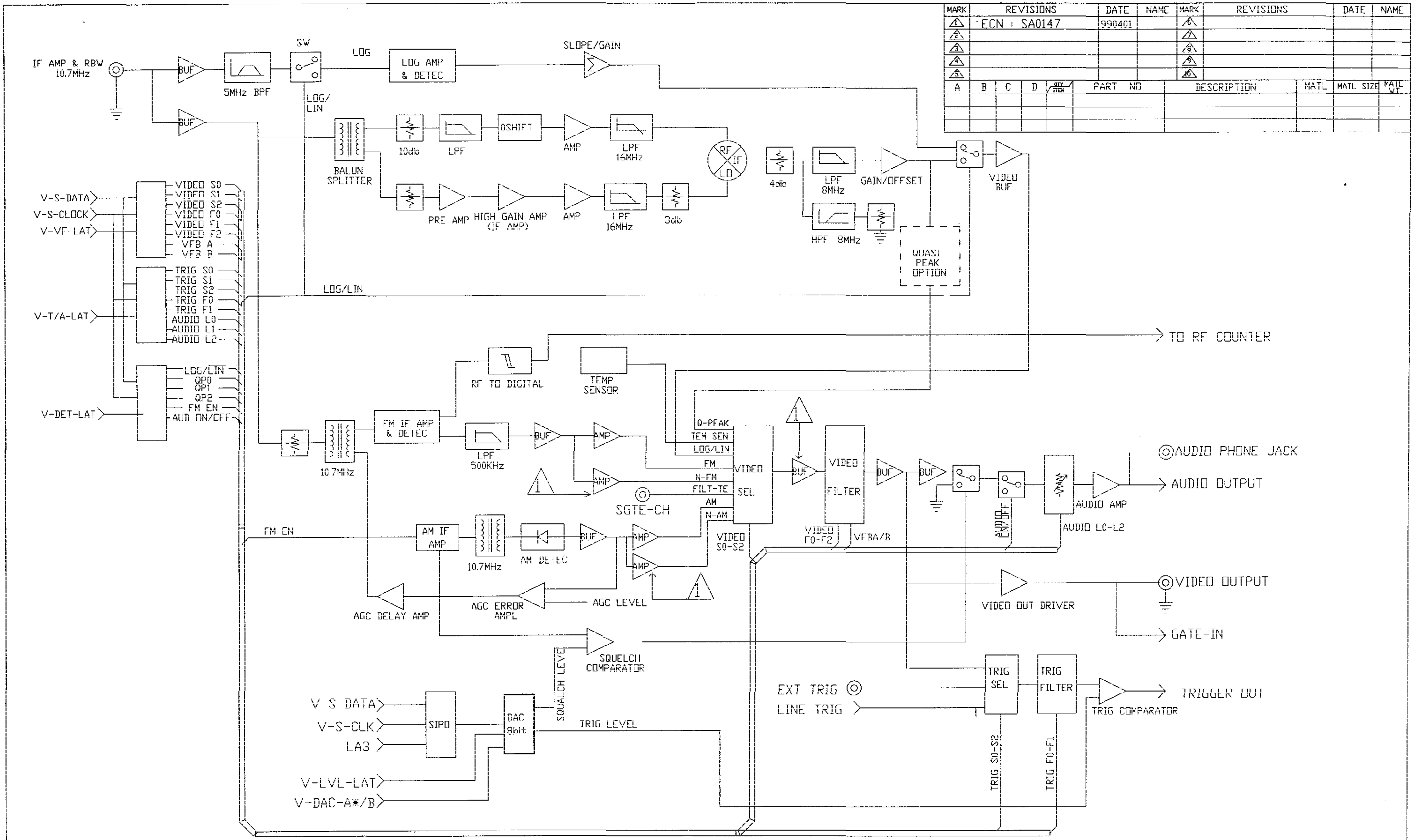

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DRAWN	990401	DATE
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VERIFIED		
APPPOVED		

TITLE
BLOCK DIAGRAM

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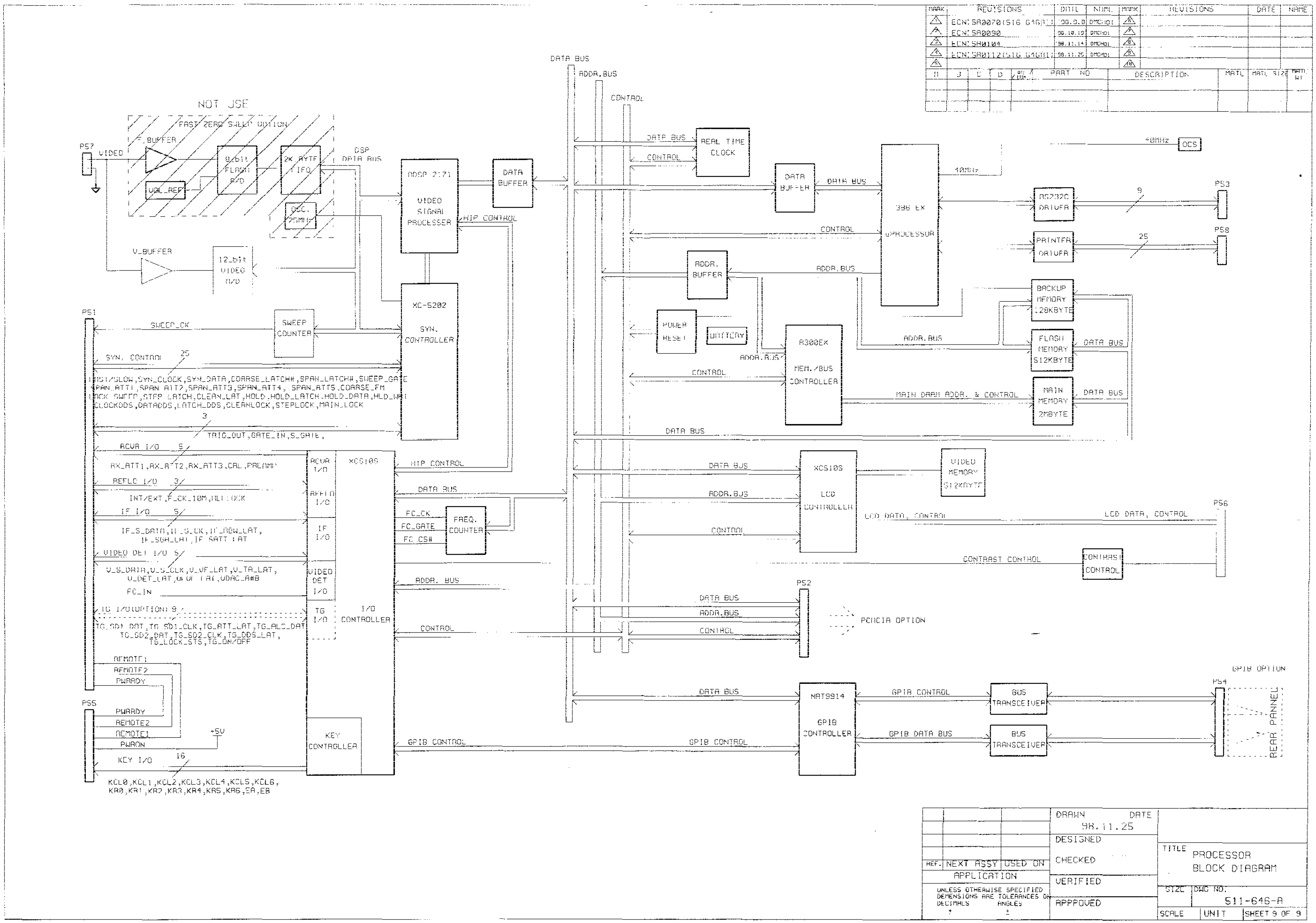
SCALE | UNIT | SHEET 7 OF 7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OSC. 20MHz
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P57
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V_BUFFER
12_bit VIDEO A/D
ADSP 2171 VIDEO SIGNAL PROCESSER
DATA BUFFER
HIP CONTROL
XC-5202 SYN. CONTROLLER
SWEEP COUNTER
SWEEP_CK
SYN. CONTROL
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TRIG_OUT,GATE_IN,S_GATE,
P51
ACVR I/O
RX_ATT1,RX_ATT2,RX_ATT3,CAL,PREAMP
REFLC I/O
INT/EXT,F_CK_10M,REFLOCK
IF I/O
IF_S_DATA,IF_S_CK,IF_ADW_LAT,
IF_SGH_LAT,IF SATT LAT
VIDEO DET I/O
V_S_DATA,V_S_CLK,V_VF_LAT,V_TA_LAT,
FC_IN
TG I/O(OPTION) 9
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TG_LOCK_STS,TG_ON/OFF
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REMOTE2
PWRRDY
P55
PWRRDY
REMOTE2
REMOTE1
PWRON
-5V
KEY I/O
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XCS10S
I/O CONTROLLER
KEY CONTROLLER
FC_CK
FC_GATE
FC_CS#
FREQ. COUNTER
DATA BUS
ADDR. BUS
CONTROL
GPIB CONTROL
REAL TIME CLOCK
ADDR. BUFFER
POWER RESET
BATTERY
R300EX MEM./BUS CONTROLLER
386 EX uPROCESSOR
40MHz
OCS
RS232C DRIVER
PRINTER DRIVER
9
P53
P58
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FLASH MEMORY 512KBYTE
MAIN MEMORY 2MBYTE
MAIN DRAM ADDR. & CONTROL
XCS10S LCD CONTROLLER
VIDEO MEMORY 512KBYTE
LCD DATA, CONTROL
P56
CONTRAST CONTROL
P52
PCMCIA OPTION
NAT9914 GPIB CONTROLLER
GPIB CONTROL
GPIB DATA BUS
BUS TRANSCEIVER
GPIB OPTION
P54
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DRAWN
DATE
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UNLESS OTHERWISE SPECIFIED DEMENSIONS ARE TOLERANCES ON DECIMALS ANGLES
TITLE
PROCESSOR BLOCK DIAGRAM
SIZE
DWG NO.
511-646-A
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UNIT
SHEET 9 OF 9

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636-003-A

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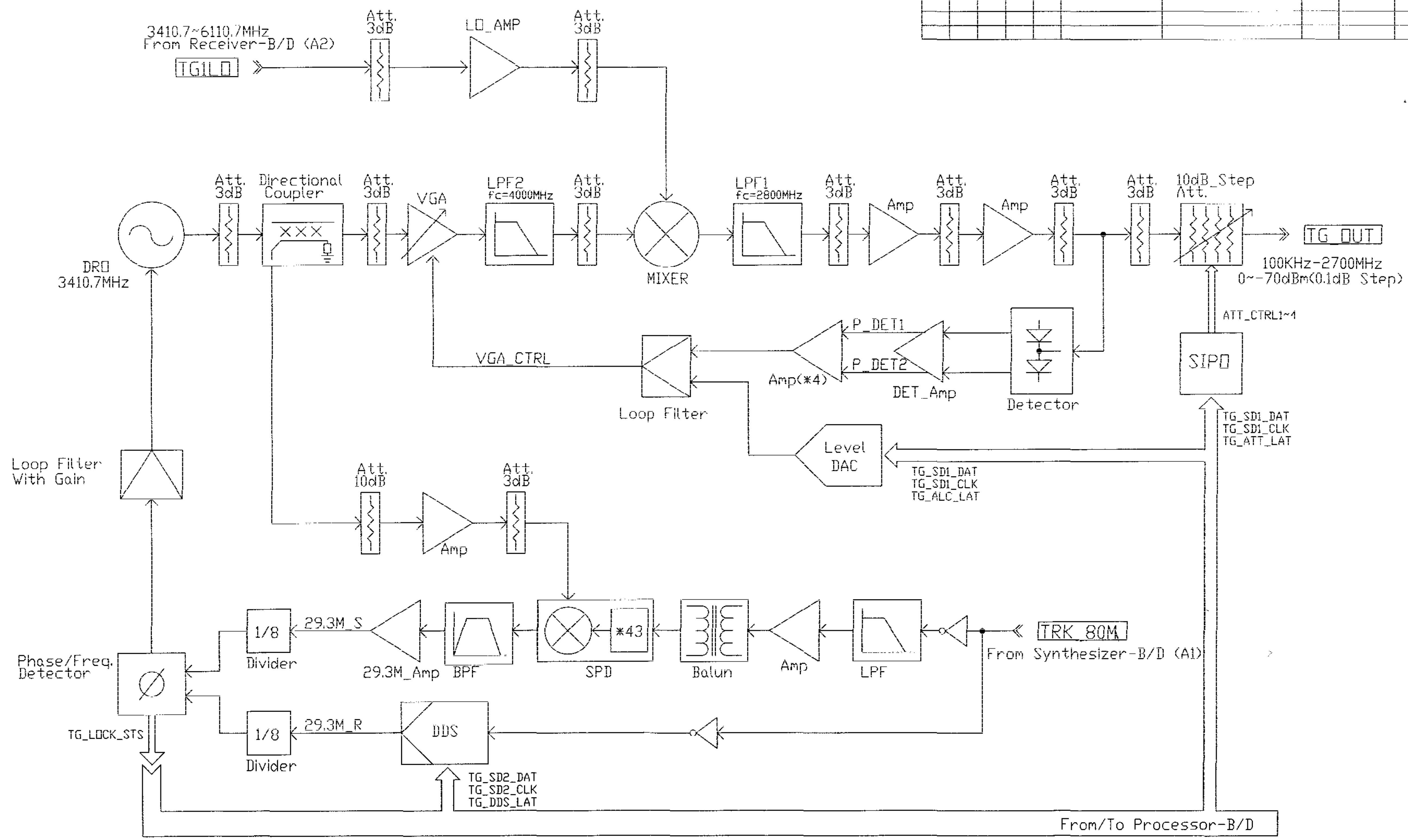

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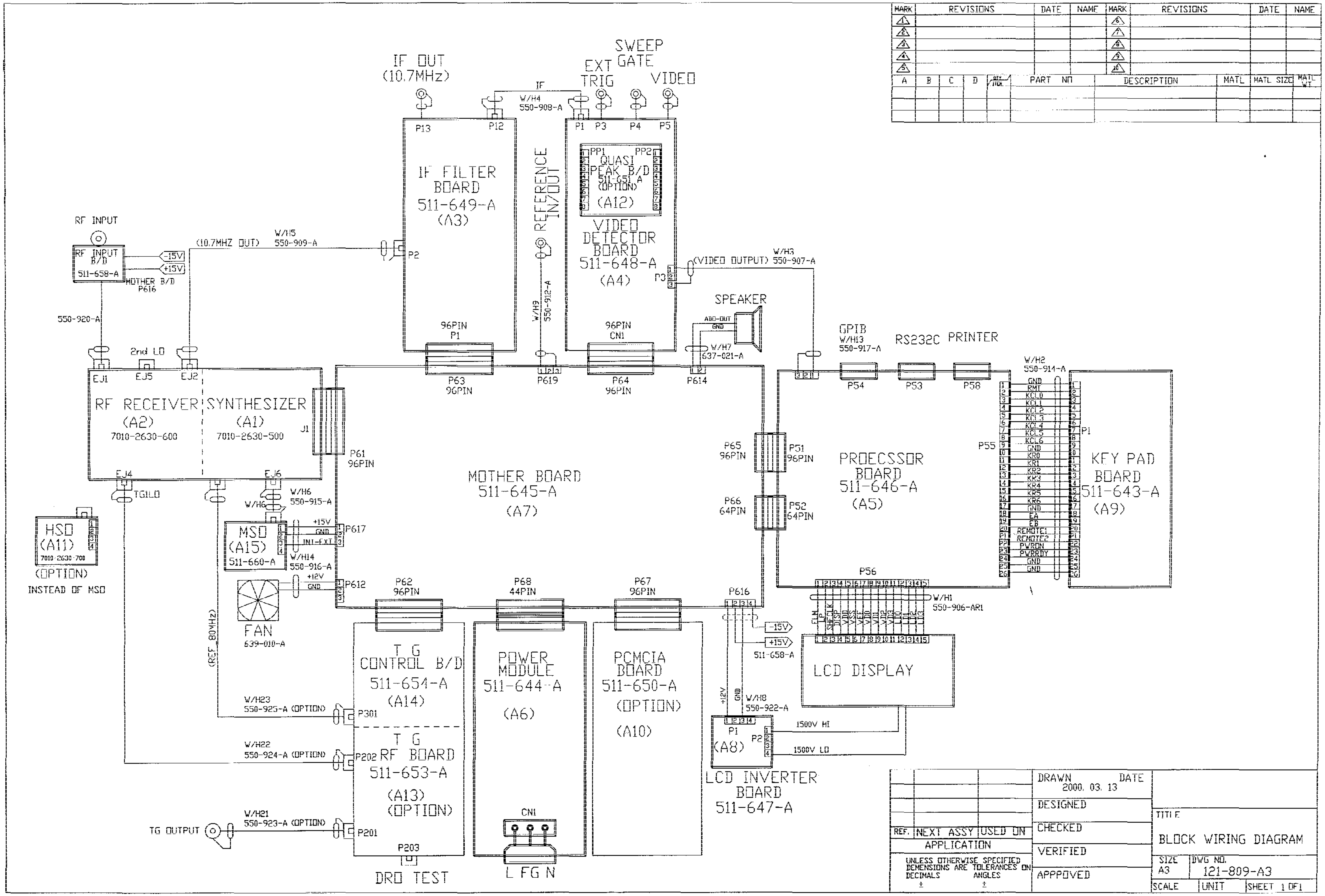
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SWEEP GATE
VIDEO
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P12
P1 P3 P4 P5
IF FILTER BOARD 511-649-A (A3)
REFERENCE IN/OUT
QUASI PEAK B/D 511-651-A (OPTION) (A12)
PP1 PP2
VIDEO DETECTOR BOARD 511-648-A (A4)
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RF INPUT B/D 511-658-A
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+15V
MOTHER B/D P616
(10.7MHZ OUT)
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P2
(VIDEO OUTPUT) W/H3 550-907-A
P3
W/H9 550-912-A
SPEAKER
ADO-OUT
GND
W/H7 637-021-A
550-920-A
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96PIN CN1
2nd LO
EJ1 EJ5 EJ2
P63 96PIN
P619
P64 96PIN
P614
GPIB W/H13 550-917-A
RS232C
PRINTER
P54 P53 P58
W/H2 550-914-A
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SYNTHESIZER (A1) 7010-2630-500
J1
P61 96PIN
MOTHER BOARD 511-645-A (A7)
P65 96PIN
P51 96PIN
P66 64PIN
P52 64PIN
PROECSSOR BOARD 511-646-A (A5)
P55
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P1
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EJ4
TGILO
EJ6
W/H6 550-915-A
HSD (A11) 7010-2630-700 (OPTION) INSTEAD OF MSD
MSD (A15) 511-660-A
+15V GND INT-EXT
P617
W/H14 550-916-A
+12V GND
P612
FAN 639-010-A
P62 96PIN
P68 44PIN
P67 96PIN
P616
P56
W/H1 550-906-AR1
-15V
+15V
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POWER MODULE 511-644-A (A6)
PCMCIA BOARD 511-650-A (OPTION) (A10)
W/H23 550-925-A (OPTION)
P301
+12V GND W/H8 550-922-A
P1 P2 (A8)
1500V HI
1500V LO
W/H22 550-924-A (OPTION)
P202
T G RF BOARD 511-653-A (A13) (OPTION)
LCD INVERTER BOARD 511-647-A
TG OUTPUT
W/H21 550-923-A (OPTION)
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P203
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DESIGNED
CHECKED
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UNLESS OTHERWISE SPECIFIED DEMENSIONS ARE TOLERANCES ON DECIMALS ANGLES
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BLOCK WIRING DIAGRAM
SIZE A3
DWG NO. 121-809-A3
SCALE UNIT SHEET 1 OF1

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Section 3

Adjustment

SECTION 3
ADJUSTMENT

TABLE OF CONTENTS

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SECTION 3 ADJUSTMENT

INTRODUCTION

Adjustment of 2398 is an automatic computer-based process that uses specially designed software. Calibration data derived from this process is saved in flash memory on the Processor Assembly.

The adjustment procedure described in this section should be performed in case of the following:

1. Any of the following modules have been changed to effect a repair:
   - RF Module Assembly
   - IF Filter and Amplifier Assembly
   - Video Detector Assembly
   - Processor Assembly
   - Tracking Generator Assembly

2. The instrument fails to meet the performance specification when tested according to the performance test procedure in the operation manual.

REQUIREMENTS

Test Equipment

1. Signal Generator *	: IFR 2042 (or 2032) or HP8648C
2. Power Meter *:	: IFR6960B or HP4418A (or 473B)
3. Power Sensor	: IFR6912 or HP8482A
4. Power Splitter	: Weinschel 1870A, IFR part no. 54311/123 [or equivalent model]
5. PC controller	: IBM Compatible [Pentium or equivalent recommended] with Microsoft Windows 95, 98 or NT Installed
6. GPIB Card	: National Instruments PCI
7. RF Cable	: N [male] to N [male], N [male] to SMB [female], BNC [male] to BNC [male]
8. GPIB Cable (qty. 2)	

* The Signal Generator and Power Meter must have GPIB interface fitted.

Test Software

Automatic test program FCAL2398 should be installed on the PC controller using the setup utility supplied. The functions of this program are as follows.

- ❑ LOG Amplifier Linearity Calibration
- ❑ IF Gain Attenuator Calibration
- ❑ RF Attenuator Calibration
- ❑ Span Attenuator Calibration
- ❑ Frequency Flatness Calibration
- ❑ Factory calibration data download / upload and serial number setting utility

A separate software utility exists for adjustment of the Tracking Generator option. This utility is called TGDAC and is a stand-alone executable program.

Main Program for Calibration

The main window of the Factory Calibration program is as shown in the figure below:

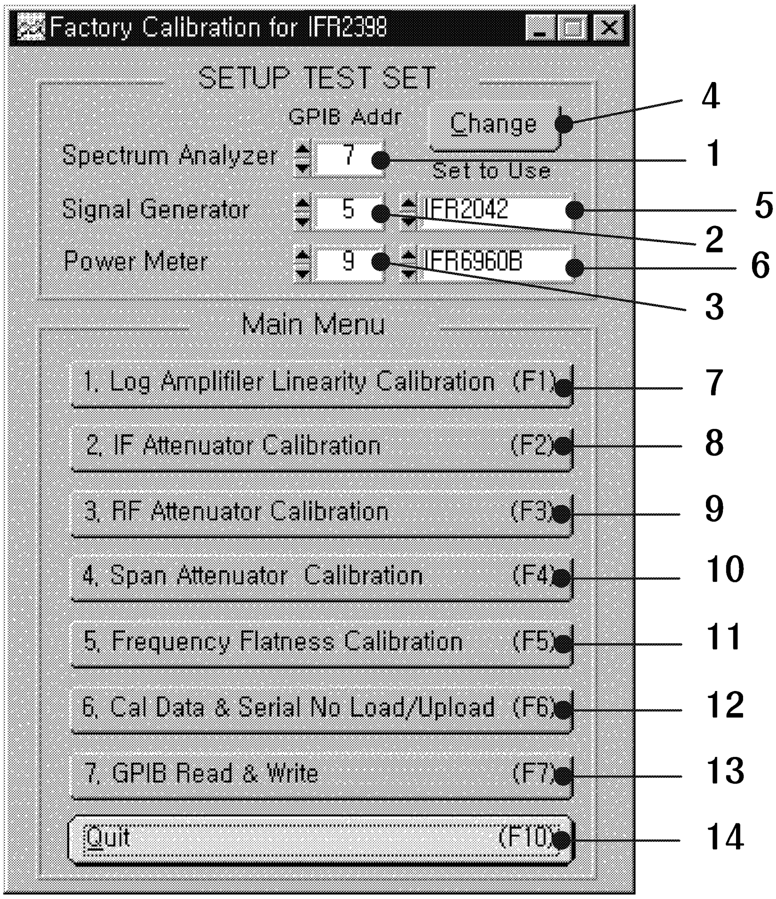

Fig. 3-1 Main window of Factory Calibration program

1. Set the GPIB address of UUT Spectrum Analyzer. Default value is 7.
2. Set the GPIB address of test equipment (Signal Generator). Default value is 5.
3. Set the GPIB address of test equipment (Power Meter). Default value is 9.
4. The GPIB addresses of UUT or test equipment are set to new value in ‘1’, ‘2’ or ‘3’. Click this button if you have changed any of the addresses.
5. Select another Signal Generator (IFR2042, HP8648C) as test equipment.
6. Select another Power Meter (IFR6960B, HP4418A(or 437B)) as test equipment.
7. When this button is selected, the sub window of Log Amplifier Linearity Calibration is displayed. The hot key is F1.

8. When this button is selected, the sub window of IF Gain Attenuator Calibration is displayed. The hot key is F2.
9. When this button is selected, the sub window of RF Attenuator Calibration is displayed. The hot key is F3.
10. When this button is selected, the sub window of Span Attenuator Calibration is displayed. The hot key is F4.
11. When this button is selected, the sub window of Frequency Flatness Calibration is displayed. The hot key is F5.
12. When this button is selected, the sub window of Cal Data & Serial No Load/upload is displayed. The hot key is F6.
13. When this button is selected, the sub window of GPIB Read & Write is displayed. The hot key is F7.
14. When this button is selected, the main program is terminated. The hot key is F10.

PREPARATION

Disassembly

To perform the adjustment procedures the cover assembly must be removed from the instrument.

CAUTION

CONTAINS PARTS AND ASSEMBLIES SUSCEPTBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

CALIBRATION PROCEDURES SHOULD ONLY BE PERFORMED IN AN ESD ENVIRONMENT. PERSONNEL PERFORMING THE PROCEDURES SHOULD KNOW ACCEPTED ESD PRACTICES.

Environment

For best results, the calibration / verification environmental conditions should be identical to the environmental conditions at the normal operating location and nominal room temperature conditions. EMI noise free conditions are needed.

Warm Up

The instrument requires 30 minutes of stabilization time after switching power on.

ADJUSTMENT PROCEDURE

Initialization

1. Existing calibration data should be deleted before performing the calibration. The calibration process will be compromised by the presence of previously stored data.

   To delete existing calibration data, perform the following key press sequence:

   SYSTEM → More 1 of 3 → More 2 of 3 → Factory Config.. → PASSWORD (key in 27329780) → Clear Cal data → RBW Clear → RX Flatness Clear → RX Atten Clear → IF Atten Clear → Log Amp Clear → All Data Clear → Return.. → Default Setting

2. ★ Set the **Auto Align** function to " OFF ":   PRESET → Auto Align → Auto Align [OFF]

3. Turn on power to the test equipment and ensure that sufficient warm-up time is allowed for both test equipment and UUT.

4. Run FCAL2398 on the PC. When the main program window is displayed, the 'Caution!' message box will be shown in the screen. Ensure that steps 1 and 2 above have been performed before clicking 'OK'.

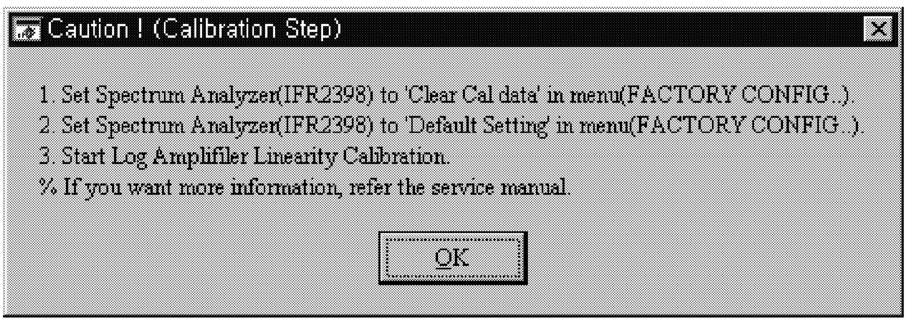

Fig. 3-2 Caution window before calibration

5. Set the GPIB address of the UUT and test equipment so that the addresses of the instruments and the addresses shown in the Factory Calibration Main Window (see page 3-5) are the same.

Log Amplifier Linearity Calibration

This calibration obtains the correct amplitude response characteristic of the log amplifier on the Video Detector Board to each RBW filter of the IF Amplifier & Filter Board.

1. Connect the test equipment and UUT as shown in the figure below:

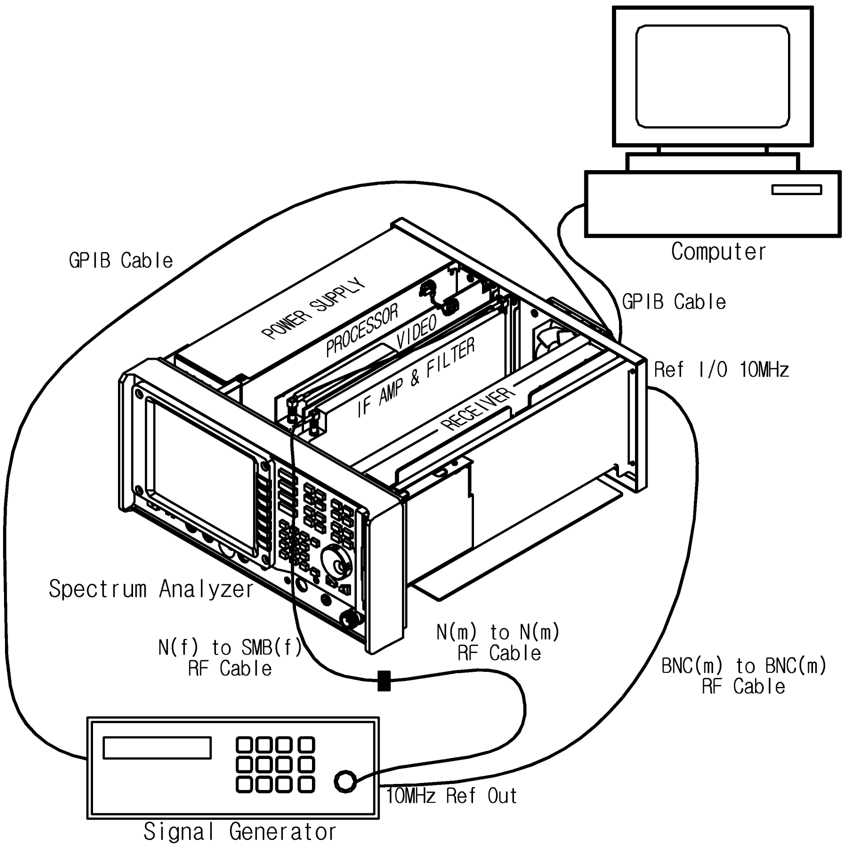

Fig. 3-3 Log Amplifier Linearity Calibration

2. Press the button 'Log Amplifier Linearity Calibration (F1)' of the main program and the following sub program window will be shown:

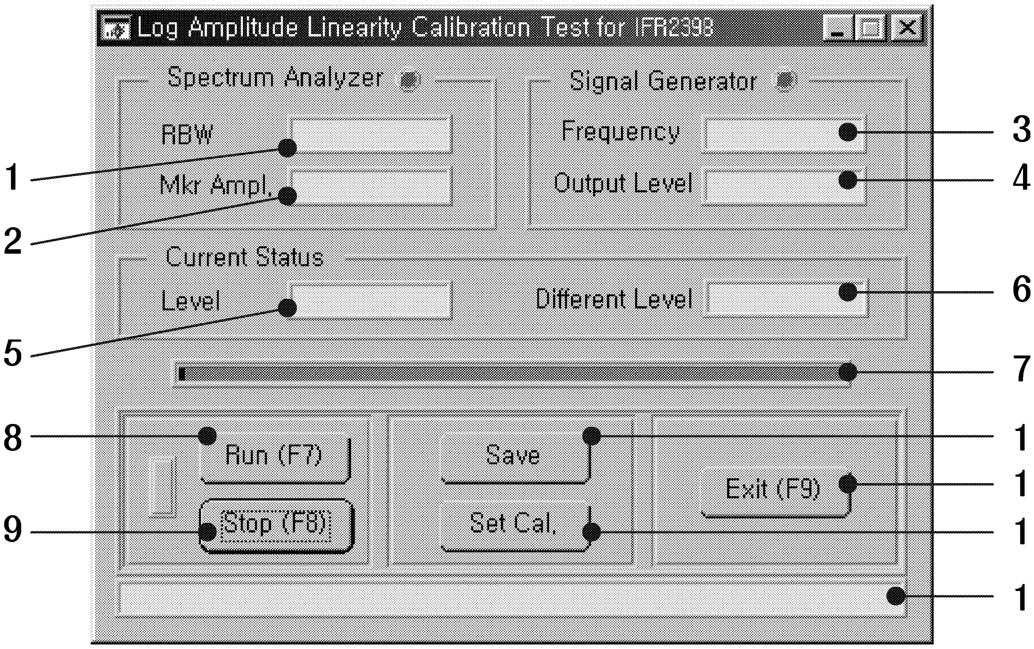

Fig. 3-4 Sub program window of Log Amplifier Linearity Calibration

- The RBW (1) value and Marker value (2) of the UUT will be shown in the Spectrum Analyzer box of sub program window.
  RBW values : 3MHz, 1MHz, 300kHz, 100kHz, 30kHz, 10kHz, 3kHz, 1kHz, 300Hz
- The Frequency (3) and Output Level (4) of the Signal Generator will be shown in the Signal Generator box of sub program window.
  Frequency : 10.7 MHz
- The Level (5) and Different Level (6) value will be shown in the Current Status box of sub program window. Different Level is a correction value for Log Amplifier Linearity.
- The Progress bar (7) and Status bar (13) will show the current state of the program.

3. Select the Run (8) button to start the calibration. (If necessary, the program can be stopped by selecting the Stop (9) button.)

4. When the program has successfully* completed the calibration, the following message box will appear:

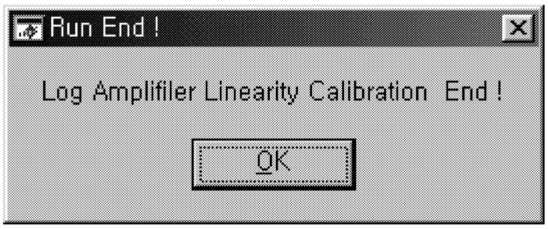

Fig. 3-5 Calibration end message box

5. Select the Set Cal. (11) button to transfer the calibration result data to the UUT.

6. (Optional) If required, a record of the calibration result data can be saved in the PC by selecting the Save (10) button.

7. Select the Exit (12) button to terminate the Log Amplifier Linearity Calibration.

* If any faults are found, “Range is Over 6 dB” message box will be shown in the screen. This message means the correction value is outside ±6dB of the standard value. This condition is regarded as an error. If the error occurs twice, the board is judged as defective.

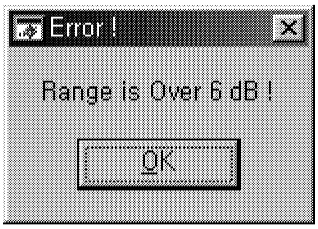

Fig. 3-6 Error message box of Log Amplifier Linearity Calibration

IF Gain Attenuator Calibration

This calibration obtains the correct amplitude response characteristic of the step gain amplifier and attenuator on the IF Filter & Amplifier Board.

1. Connect the test equipment and UUT as shown in the figure below:

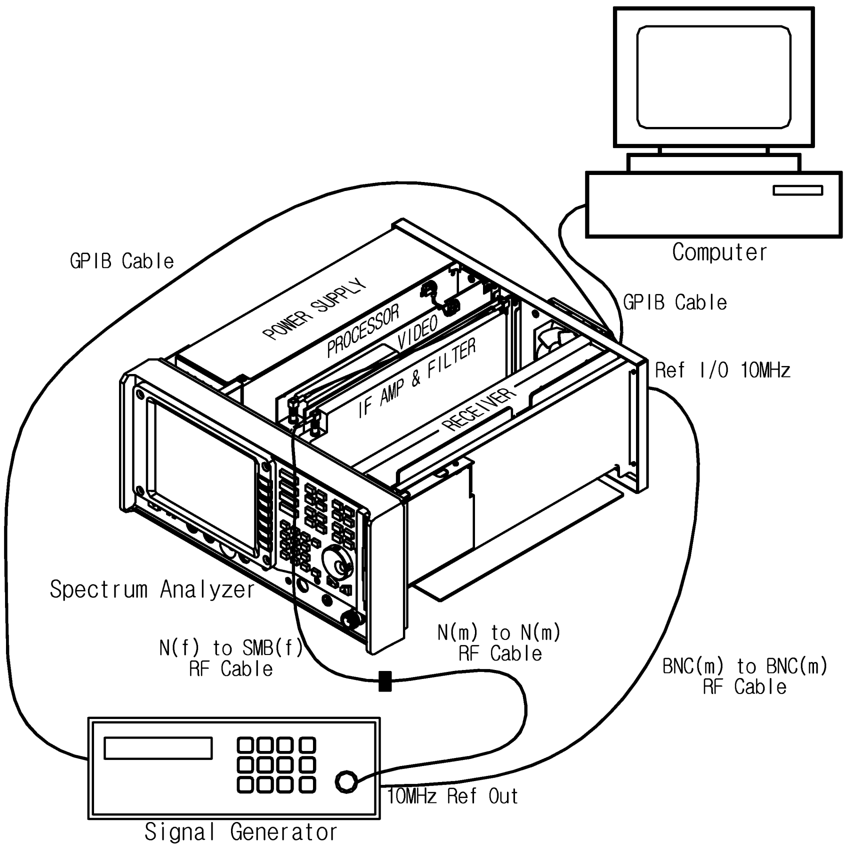

Fig. 3-7 IF Gain Attenuator Calibration

2. Press the 'IF Attenuator Calibration (F2)' of the main program and the following sub program window will be shown:

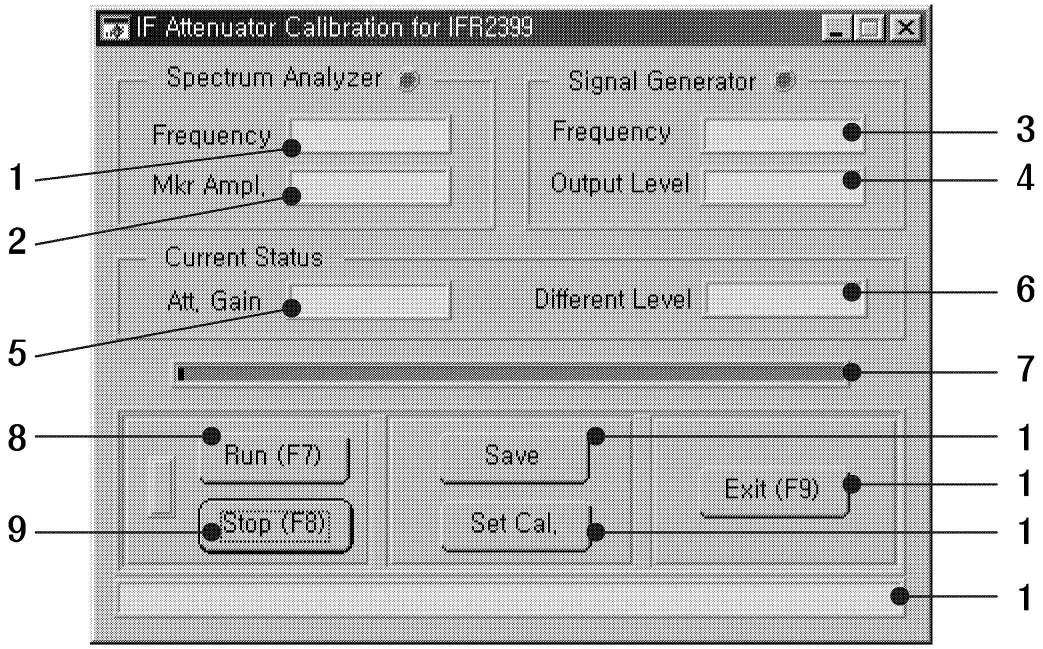

Fig. 3-8 Sub program window of IF Gain Attenuator Calibration

- The Frequency (1) value and Mkr Ampl (2) of the instrument will be shown in the Spectrum Analyzer box of sub program window.
  Frequency : 1450MHz
- The Frequency (3) and Output Level (4) of the Signal Generator will be shown in the Signal Generator box of sub program window.
  Frequency : 10.7MHz
- The Att. Gain (5) and Different Level (6) will be shown in the Current Status box of sub program window. Different Level is a correction value for IF Gain Attenuator.
  IF Gain Attenuator : 1, 2, 4, 8, 10, 20_1, 20_2 dB
- The Progress bar (7) and Status bar (13) will show the current state of the program.

3. Select the Run (8) button in the sub program window using the mouse in order to start calibration. (If necessary, the program can be stopped by selecting the Stop (9) button.)

4. When the program has successfully* completed the calibration, the following message box will appear:

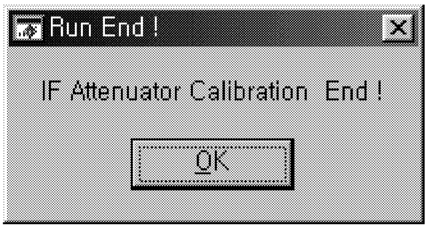

Fig. 3-9 Calibration end message box

5. Select the Set Cal (11) button to transfer the calibration result data to the UUT.

6. (Optional) If required, a record of the calibration result data can be saved in the PC by selecting the Save (10) button.

7. Select the Exit (12) button to terminate the IF Attenuator Calibration.

* If any faults are found, "Range is Over 1 dB" message box will be shown in the screen. This message means the correction value is outside ±1dB of the standard value. This condition is regarded as an error. If the error occurs twice, the board is judged as defective.

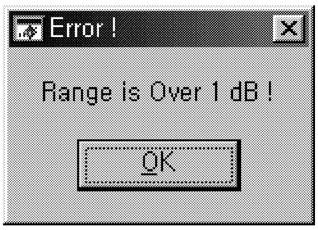

Fig. 3-10 Error message box of IF Gain Attenuator Calibration

RF Attenuator Calibration

This calibration obtains the correct amplitude response characteristic of the RF input step attenuator.

1. Connect the UUT as shown in the figure below:

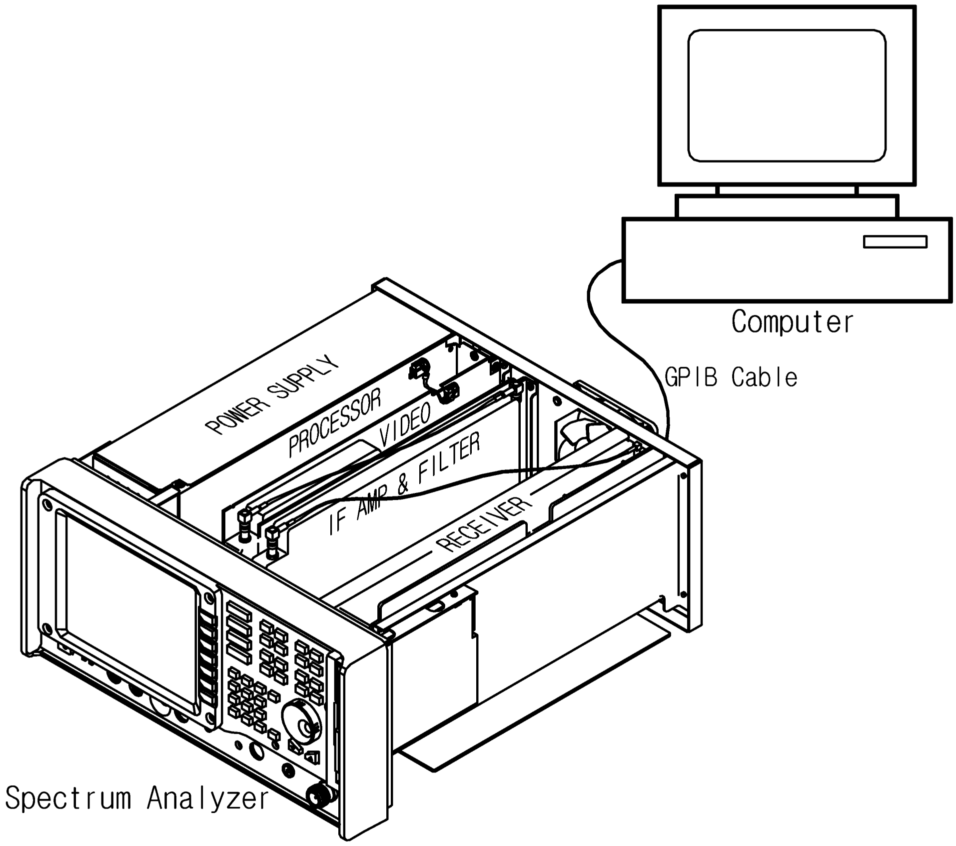

Fig. 3-11 RF Attenuator Calibration

2. Press the button 'RF Attenuator Calibration (F3)' of the main programs and the following sub program window will be shown:

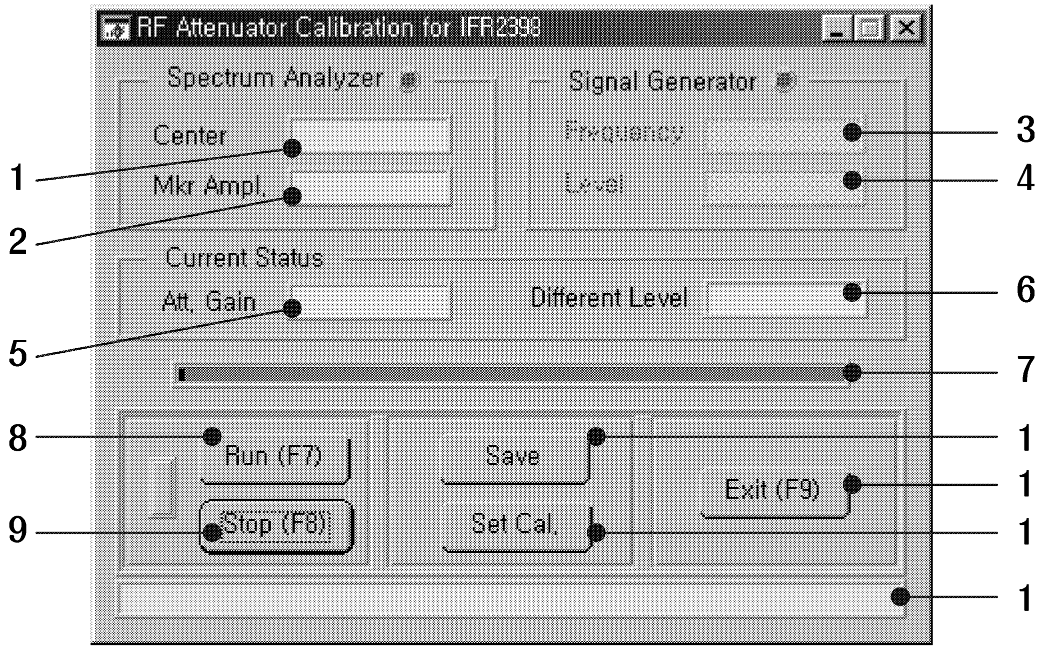

Fig. 3-12 Sub program window of RF Attenuator Calibration

- The Center (1) value and Mkr Ampl (2) value of the UUT will be shown in the Spectrum Analyzer box of sub program window.
  Frequency : 40 MHz
- The Frequency (3) and Output Level (4) in the Signal Generator box of the sub program window are blank, since the Signal Generator is not used.
- The Att. Gain (5) and Different Level (6) will be shown in the Current Status box of sub program window. Different Level is a correction value for the RF Attenuator.
  RF Attenuator : 0, 10, 20, 30, 40, 50 dB
- The Progress bar (7) and Status bar (13) will show the current state of the program.

3. Select the Run (8) button in the sub program window using the mouse in order to start calibration. (If necessary, the program can be stopped by selecting the Stop (9) button.)

4. When the program has successfully* completed the calibration, the following message box will appear:

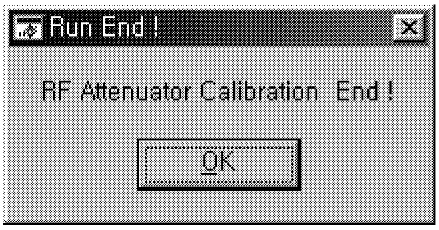

Fig. 3-13 Calibration end message box

5. Select the Set Cal. (11) button to transfer the calibration result data to the UUT.

6. (Optional) If required, a record of the calibration result data can be saved in the PC by selecting the Save (10) button.

7. Select the Exit (12) button to terminate the RF Attenuator Calibration.

* If any faults are found, "Range is Over 1 dB" message box will be shown in the screen. This message means the correction value is outside ±1dB of the standard value. This condition is regarded as an error. If the error occurs twice, the board is judged as defective.

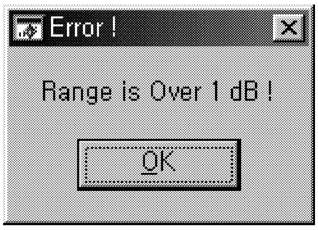

Fig. 3-14 Error message box of RF Attenuator Calibration

Span Attenuator Calibration

This calibration obtains the correct the frequency range of the Synthesizer in the RF Module. It compensates for the tolerance of the resistor used in the Span Adjusting Attenuator.

1. Connect the test equipment and UUT as shown in the figure below:

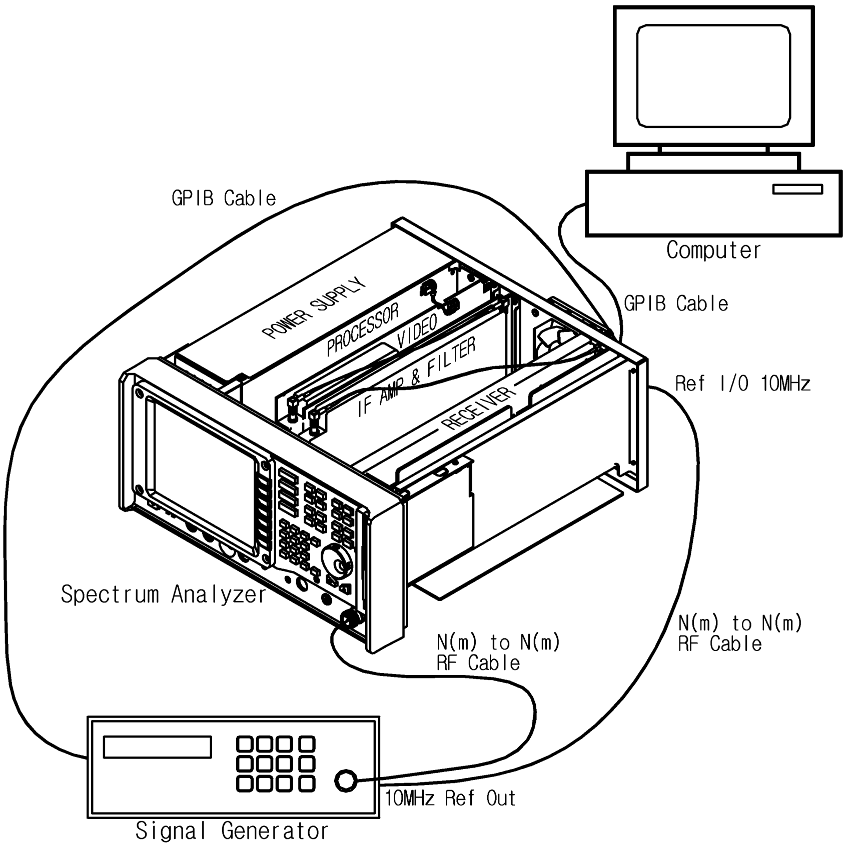

Fig. 3-15 Span Attenuator Calibration

2. Press the button ‘Span Attenuator Calibration (F4)’ in the main program window and the following sub program window will be shown:

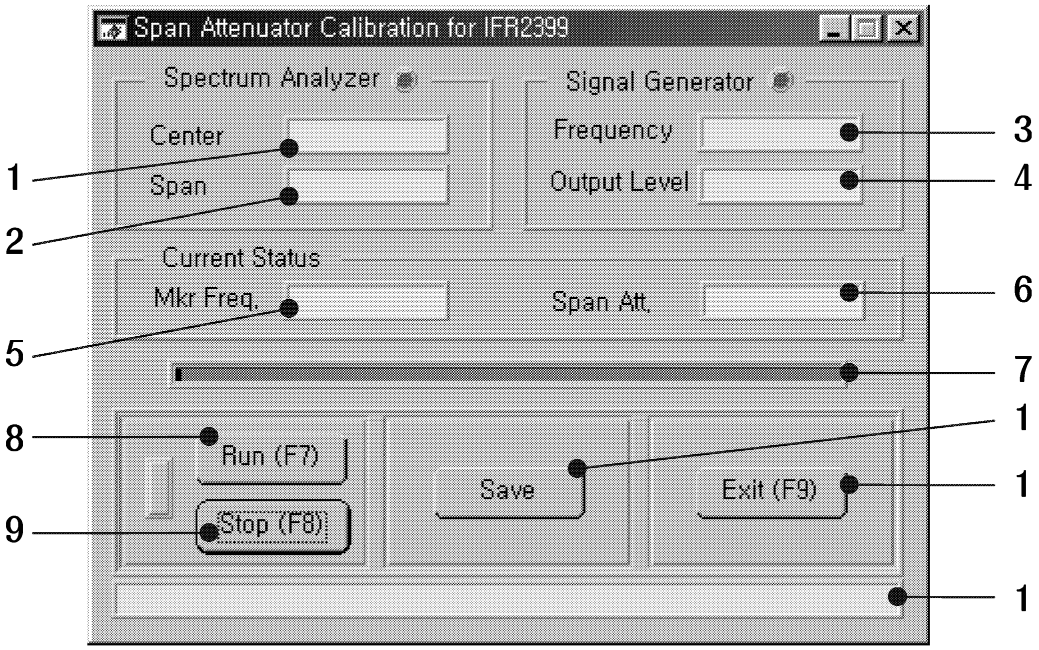

Fig. 3-16 Sub program window of Span Attenuator Calibration

- The Center (1) value and Span (2) value of the UUT will be shown in the Spectrum Analyzer box of sub program window.
  Center Frequency : 1450MHz
  Span Frequency : 20, 50, 100, 200, 500, 1000, 2000, 2900MHz
- The Frequency (3) and Output Level (4) of the Signal Generator will be shown in the Signal Generator box of sub program window.
- The Mkr Freq. (5) and Span Att (6) value will be shown in the Current Status box of sub program window. Span Att is a correction value for Span Attenuator. Default correction value of Span Attenuator is '1.0' and is adjusted in 0.01 steps. The correction data is transferred to the UUT automatically.
- The Progress bar (7) and Status bar (12) will show the current state of the program.

3. Select the Run (8) button to start the calibration. (If necessary, the program can be stopped by selecting the Stop (9) button.)

4. When the program has successfully* completed the calibration, the calibration data will be automatically transferred to the UUT.

5. (Optional) If required, a record of the calibration result data can be saved in the PC by selecting the Save (10) button.

6. Select the Exit (11) button to terminate the Span Attenuator Calibration.

* If any faults are found, “Range is Over” message box will be shown in the screen. This message means the correction value is outside the control range of the standard value. This condition is regarded as an error. If the error occurs twice, the board is judged as defective.

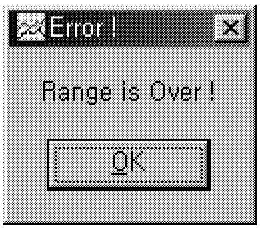

Fig. 3-17 Error message box of Span Attenuator Calibration

Frequency Flatness Calibration

This calibration obtains correction for the level errors for each attenuator setting over the frequency range of the instrument.

1. Connect the Power Sensor to the Power Meter via the power sensor cable. Connect the Sensor to the Power Reference connector on the Power Meter. If using the IFR 6960B Power Meter, enter the Sensor's Lin Factor and Cal Factor into the Power Meter. Zero and Calibrate the Power Sensor.

2. Execute the **Auto Align** function on the UUT: PRESET → Alignment Mode.. → All Align

3. Connect the test equipment and UUT as shown in the figure below:

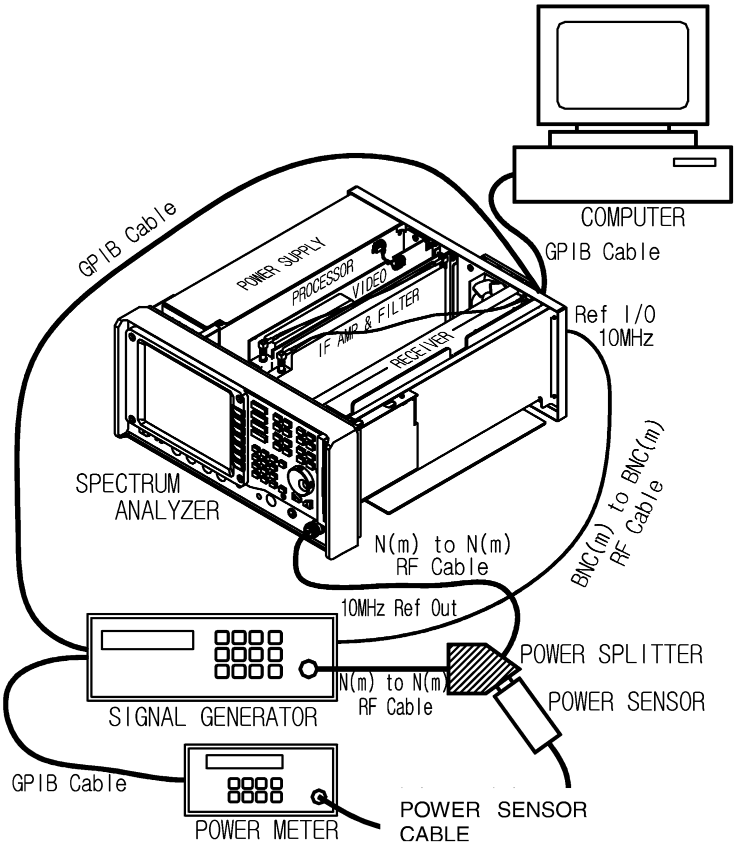

Fig. 3-18 Frequency Flatness Calibration

4. Press the button 'Frequency Flatness Calibration (F5)' in the main program window and the following caution window will be shown. Ensure that steps 1 and 2 above have been performed before clicking the OK button.

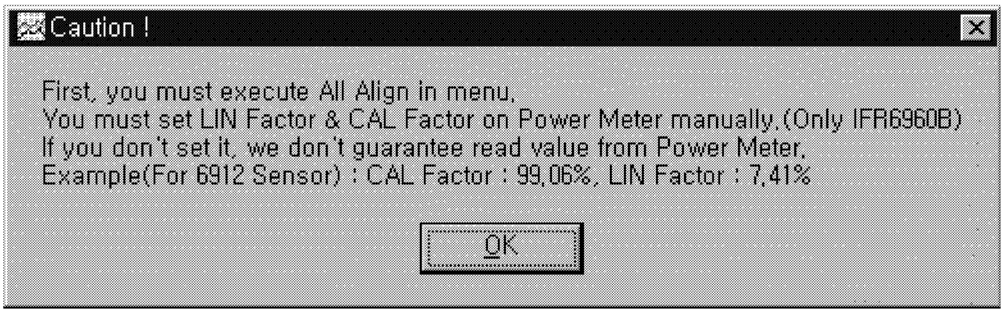

Fig. 3-19 Caution window before calibration

5. The following sub program window will now be shown:

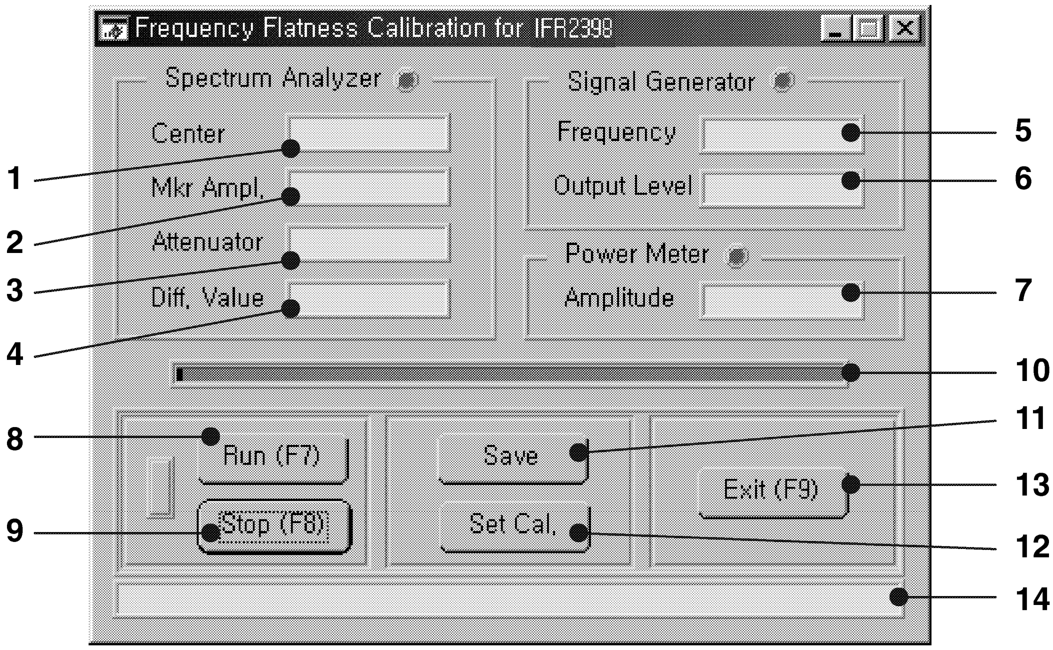

Fig. 3-20 Sub program of Frequency Flatness Calibration

- The Center (1) value, Mkr Ampl (2) value, Attenuator (3) value and Different Value (4) of the UUT will be shown in the Spectrum Analyzer box of the sub program window.
  Center Frequency:
  10kHz ~ 90kHz (every 10 kHz increment)
  100kHz ~ 900kHz (every 100 kHz increment)
  1MHz ~ 9MHz (every 1 MHz increment)
  10MHz ~ 2900MHz (every 10 MHz increment)
  Attenuator : 0, 10, 20, 30, 40, 50dB
  Different Value is a correction value for Frequency Flatness.
- The Frequency (5) and Output Level (6) of the Signal Generator will be shown in the Signal Generator box of sub program window. Frequency is the same as the Center Frequency of the UUT.
- The Amplitude (7) value will be shown in the Power Meter box of sub program window. Amplitude is the value measured by the Power Meter.
- The Progress bar (10) and Status bar (14) will show the current state of the program.

6. Select the Run (8) button to start the calibration. (If necessary, the program can be stopped by selecting the Stop (9) button.

7. Select the Set Cal. (11) button to transfer the calibration result data to the UUT.

8. (Optional) If required, a record of the calibration result data can be saved in the PC by selecting the Save (10) button.

9. Select the Exit (12) button to terminate the Frequency Flatness Calibration.

Tracking Generator Calibration (Option)

This calibration obtains the correct amplitude response characteristic of the Tracking Generator in steps of 0.1dB and 1dB. The DAC code data range is between 0 to 4095, with standard DAC codes as follows:

ID number	Level	DAC Standard Code Data
0	1.0 dBm	3650
1	0.0 dBm	3174
2	-1.0 dBm	2760
3	-2.0 dBm	2393
4	-3.0 dBm	2068
5	-4.0 dBm	1783
6	-5.0 dBm	1533
7	-6.0 dBm	1311
8	-7.0 dBm	1118
9	-8.0 dBm	949
10	-9.0 dBm	800
11	-10.0 dBm	670
12	-11.0 dBm	559
13	0.9 dBm	3600
14	-10.9 dBm	569

1. Connect the test equipment and UUT as shown in the figure below:

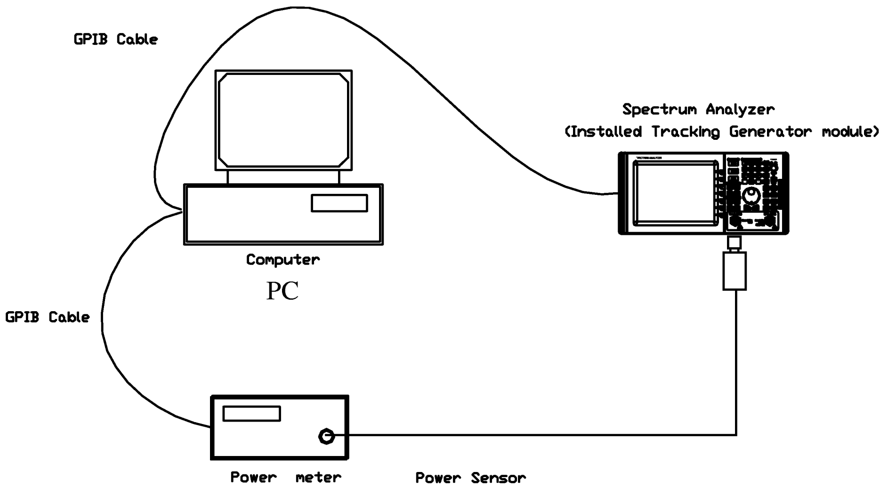

Fig. 3-21 Tracking Generator Calibration

2. Execute the file named “TGDAC.EXE”. A caution message box will appear indicating that the equipment requires 30 minutes of warm-up time after switching power on. Click the “YES” button to go on to the next step and the following window will be shown. Clicking the “NO” button will cancel the calibration.

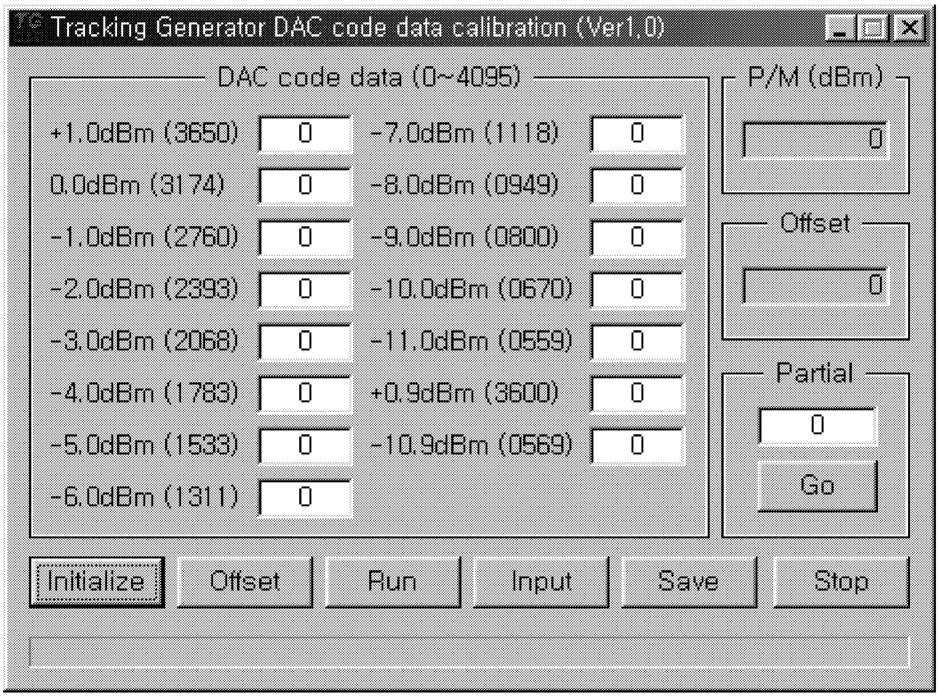

Fig. 3-22 Program window of Tracking Generator Calibration

3. Select the “INITIALIZE” button to initialize the program. When “Initialized” is shown in the screen, click the “OK” button to go on to the next stage.

4. Select the “OFFSET” button. This step measures the difference between the level set on the tracking generator and the measured absolute value.

5. Select the “RUN” button to continue the calibration. When “Measurement Completed” is shown in the screen, click the “OK” button to go on to the next stage.

6. Select the "INPUT" button to transfer the calibration data to the UUT. A message box stating “Input Completed” will appear when complete *.

7. (Optional) If required, a record of the calibration result data can be saved in the PC by selecting the “SAVE” button

8. Select the "STOP" button to quit the Program Window after completing the Tracking generator DAC code calibration.

* If any faults are found, “Over range of DAC code. Stop program” will be shown in the screen. This message means the correction DAC code data range of 0 to 4095 has been exceeded. This is regarded as an error and the program will stop.

Fig. 3-23 DAC Code over-range message box

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CALIBRATION DATA BACKUP & SERIAL NUMBER SET PROCEDURE

The following procedure describes the method for uploading the 2398's calibration data into a PC (running Windows 9x), for downloading the calibration data from the PC into the instrument and for saving and retrieving a backup data file on the PC. The software utility required is part of the Factory Calibration package, FCAL2398. This utility is also used to upload and download the instrument serial number.

It is important to follow this procedure carefully in order to avoid accidental loss of data, which may result in malfunction of the instrument. Read through this procedure in full before performing any of the functions of this utility.

1. Set the GPIB Address of the 2398 to be the same as set in the Factory Calibration Main Window, Fig. 3-1 (default value 7).
2. ★ Set the **Auto Align** function to " OFF ":

   PRESET → Auto Align → Auto Align [OFF]
3. In the Factory Calibration Main Window, press the button 'Cal Data & Serial No Load/Upload (F6)' and the following sub program window will be shown:

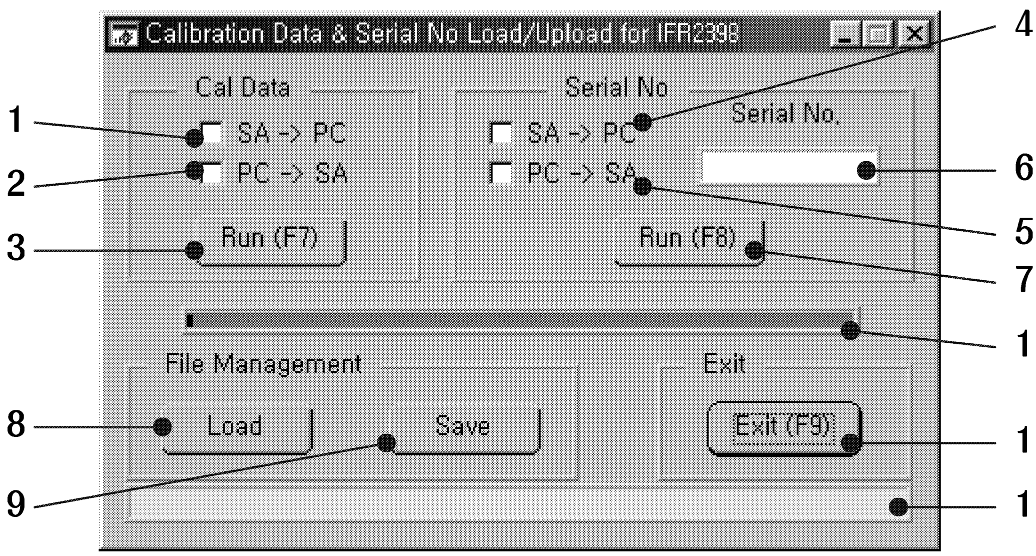

Fig. 3-24 Sub program window of calibration data load/upload & S/N set

4. Upload the Serial Number

- To upload the serial number of the instrument, select the SA -> PC (4) check box in the sub program window, then select the Run (7) button.

Fig. 3-25 Load the serial number

- The serial number of instrument will be displayed in the Serial No. (6) edit box after about 1 second.
- The following status message in the Status bar (12) will be shown.

Fig. 3-26 Load completed message

5. Download the Serial Number

- To download the serial number into the instrument, select the PC -> SA (5) check box in the sub program window. Enter the correct serial number (up to 8 characters) in the Serial No. (6) edit box, then select the Run (7) button.

Fig. 3-27 Load the serial number

- The following status message in the Status bar (12) will be shown.

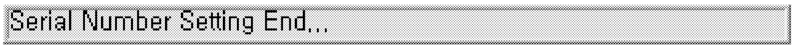

Fig. 3-28 Load completed message

6. Upload calibration data

- To upload the calibration data, select the SA -> PC (1) check box in the sub program window, then select the Run (3) button.

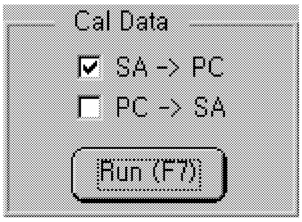

Fig. 3-29 Upload the factory calibration data

- The following status messages in the Status bar (12) will be shown during, and following the completion of, the upload.

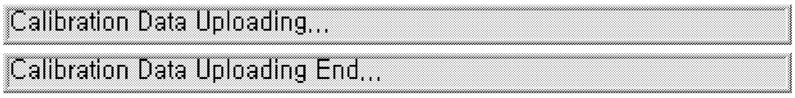

Fig. 3-30 Upload message

7. Download calibration data

- To download the calibration data, select the PC -> SA (2) check box in the sub program window, then select the Run (3) button.

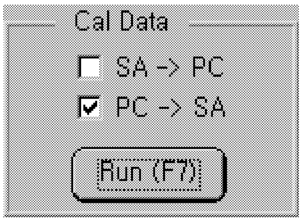

Fig. 3-31 Load the factory calibration data

- The following status messages in the Status bar (12) will be shown during, and following the completion of, the download.

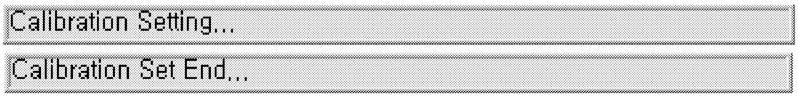

Fig. 3-32 Load message

8. Save the calibration data to a file in the PC

- Select the Save (9) button in the File Management box of the sub program window to save the calibration data and serial number to file in the PC.
- The structure of the file will be as shown in Fig. 3-33.

9. Retrieve a saved calibration data file from the PC

- Select the Load (8) button in the File Management box of the sub program window to retrieve a file containing the calibration data and serial number from the PC.
- *The data in the instrument will be different from the saved file if a calibration has been performed more recently*.
- The structure of the file will be as shown in Fig. 3-33.

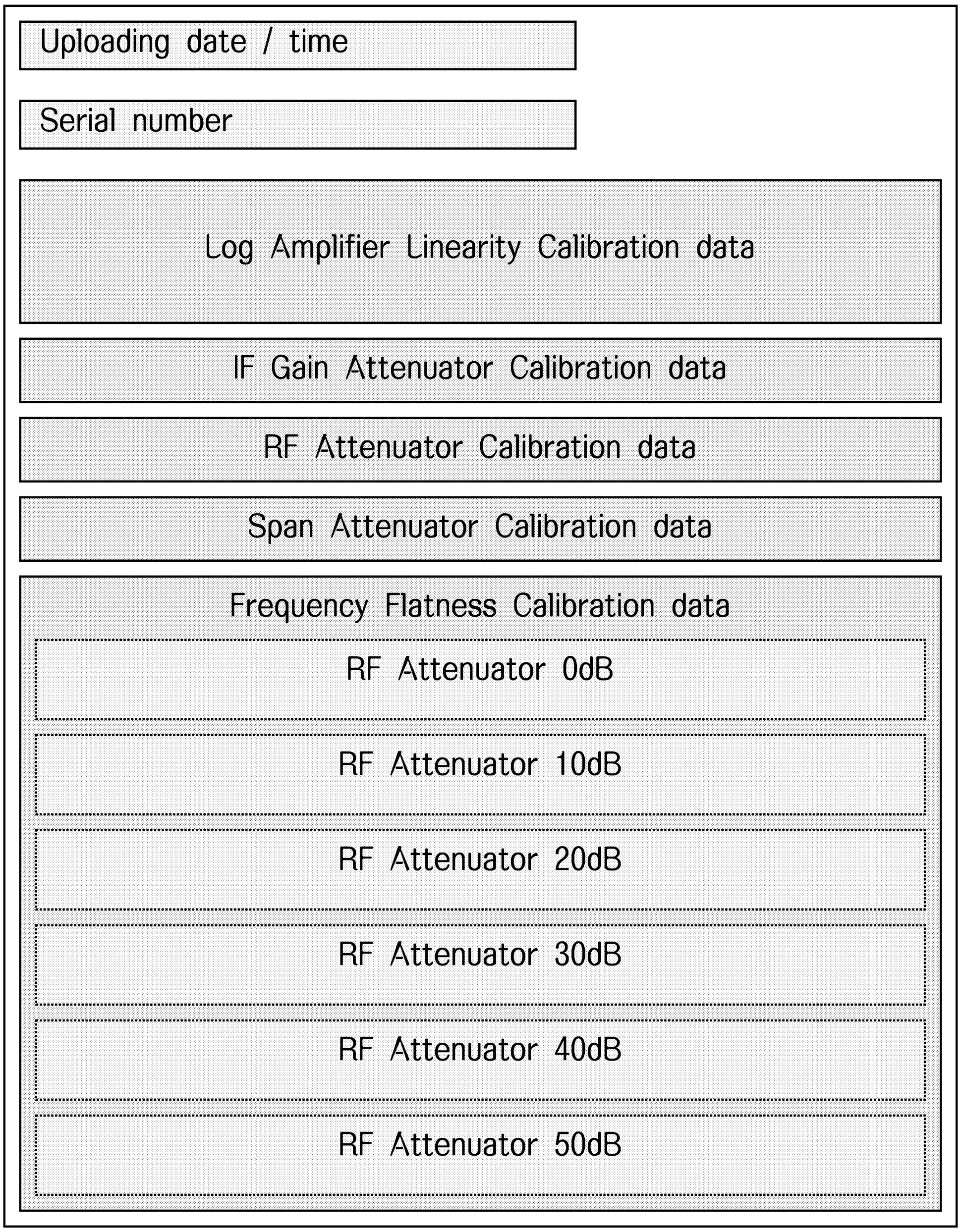

Fig. 3-33 File structure

10. Select the Exit (11) button in the sub program window to terminate the Cal Data & Serial No Load/Upload.

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Section 4

Fault Diagnosis

SECTION 4
FAULT DIAGNOSIS

This section contains instruction for diagnosis of faults on the 2398. The aim of this information is to diagnose faults to module level. Refer to applicable wiring drawings in Section 1 and Section 7 to verify cable location if necessary. Refer to Section 5 for replacement procedures for all modules.

TABLE OF CONTENTS

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SECTION 4
INTRODUCTION

CAUTION : TO AVOID DAMAGE WHEN REMOVING A SEMI-RIGID COAXIAL CABLE, LOOSEN THE CONNECTORS AT BOTH ENDS FIRST BEFORE FULLY DISCONNECTING AT EITHER END.

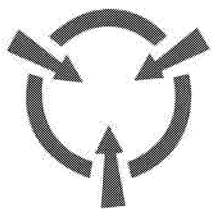
- **Safety Precautions**

  Power should be removed from the unit before any replacement procedure is initiated.

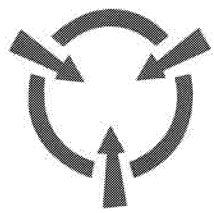
  CAUTION : **DANGEROUS VOLTAGES ARE PRESENT WITH CASE ASSEMBLIES REMOVED IF POWER IS PRESENT.**

- **ESD**

  CAUTION : THE REPLACEMENT PROCEDURES FOR THE SEPECTRUM ANALYZER SHOULD ONLY BE PERFORMED IN AN ESD ENVIRONMENT AND ALL PERSONNEL PERFORMING THE REPLACEMENT PROCEDURES SHOULD HAVE KNOWLEDGE OF ACCEPTED ESD PRACTICES AND/OR BE ESD CERTIFIED.

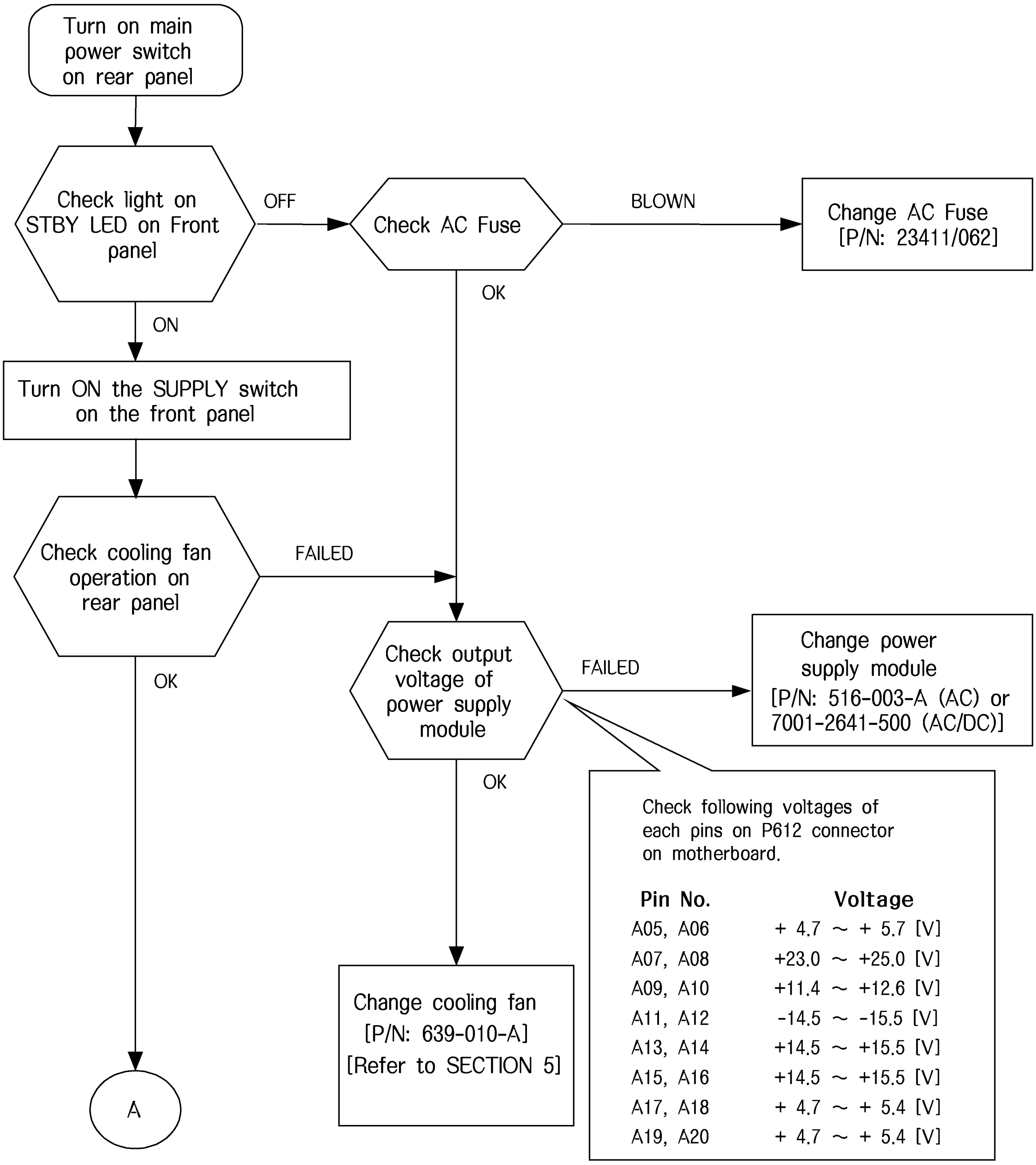


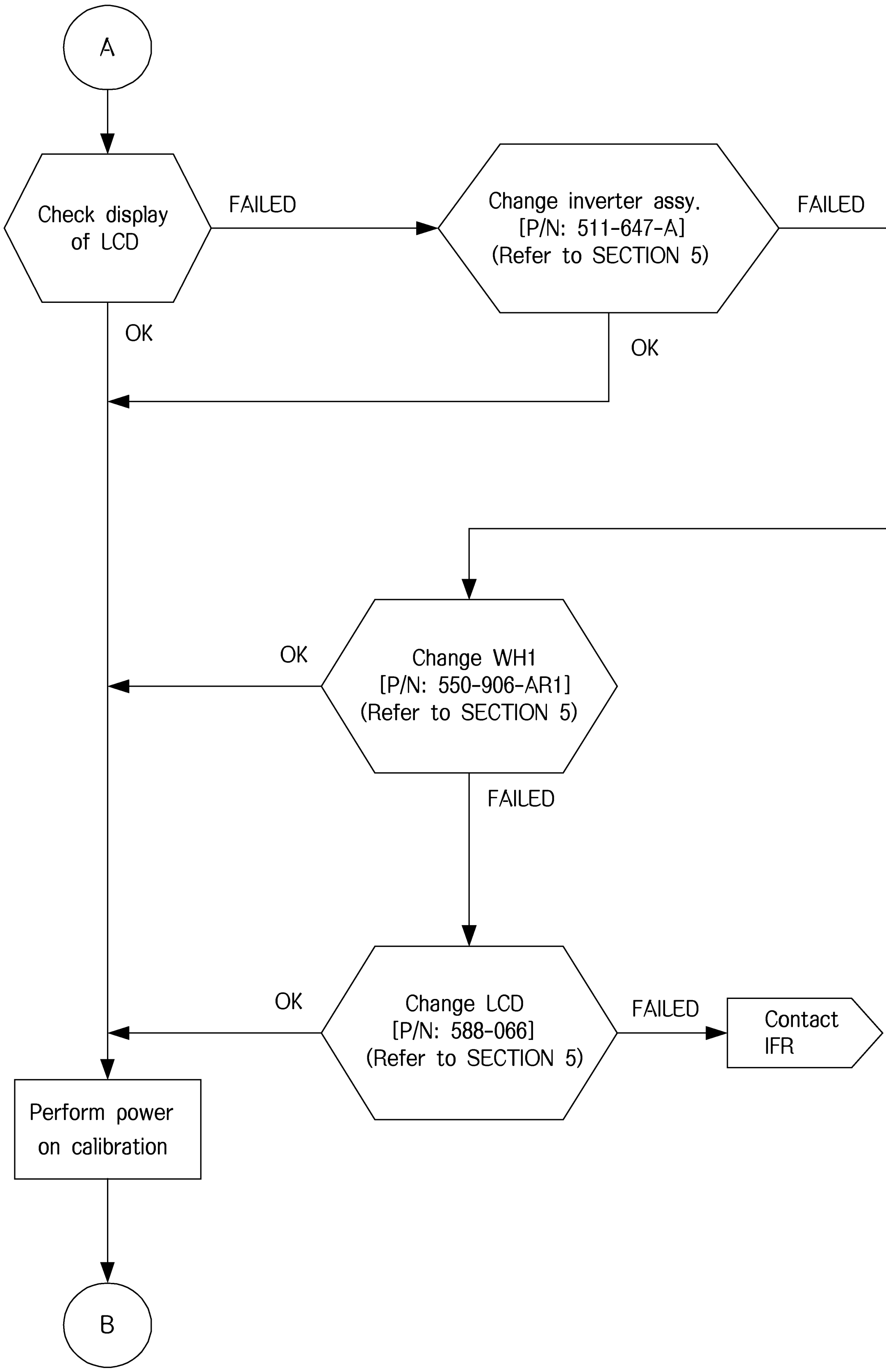
CAUTION : CONTAINS PARTS AND ASSEMBLIES SUSCEPTBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

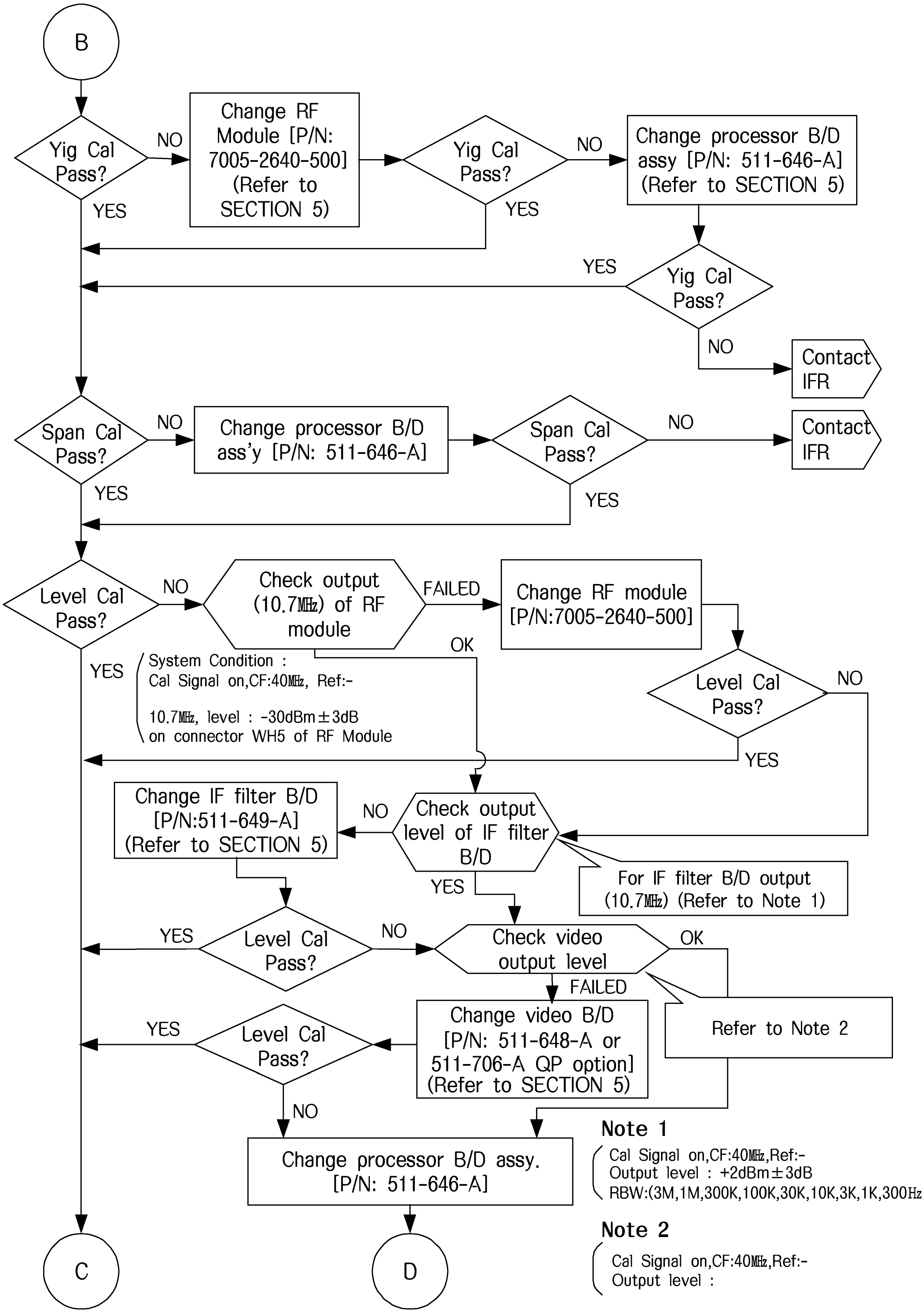


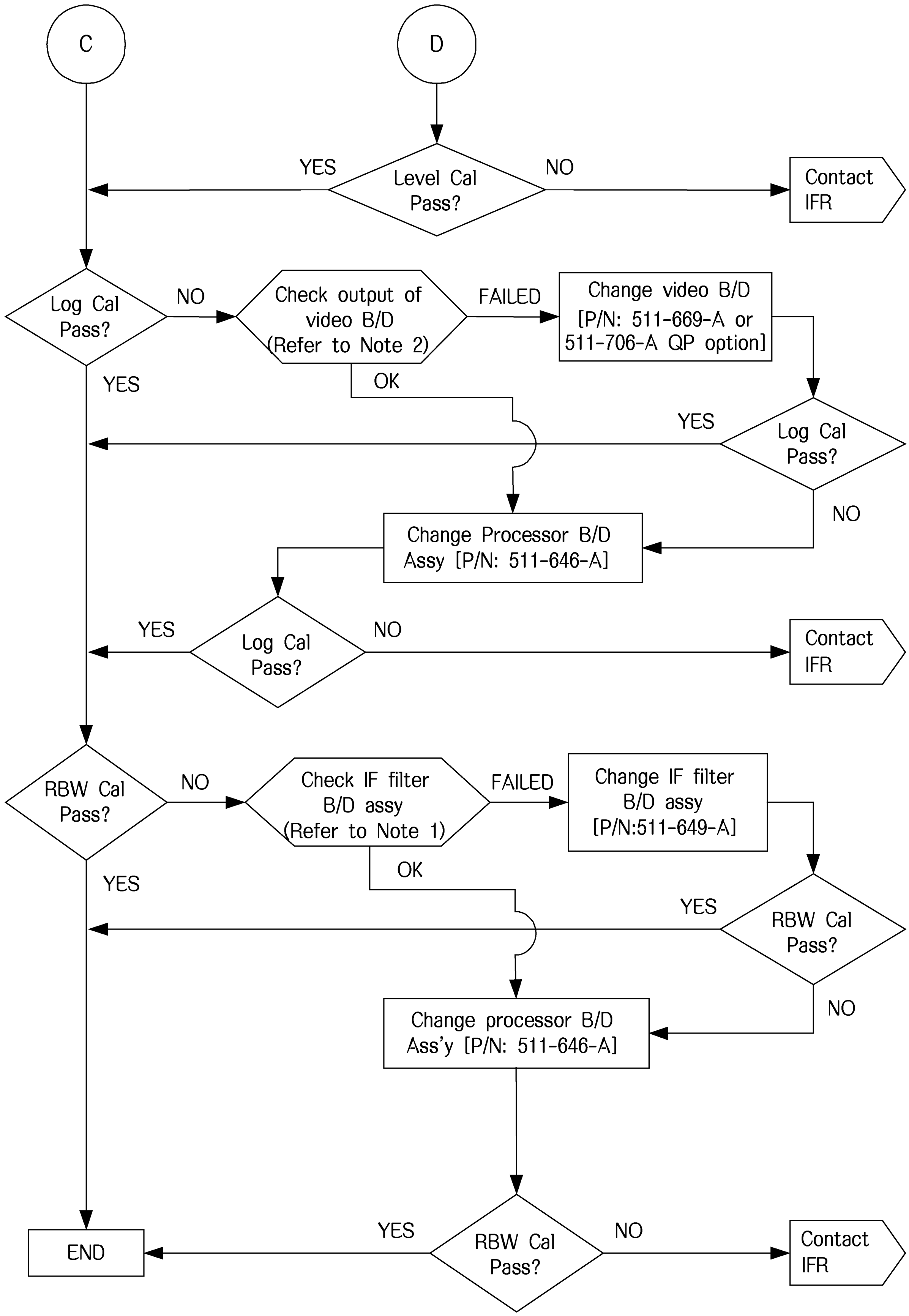
FAULT DIAGNOSIS

Fault diagnosis procedure for 2398



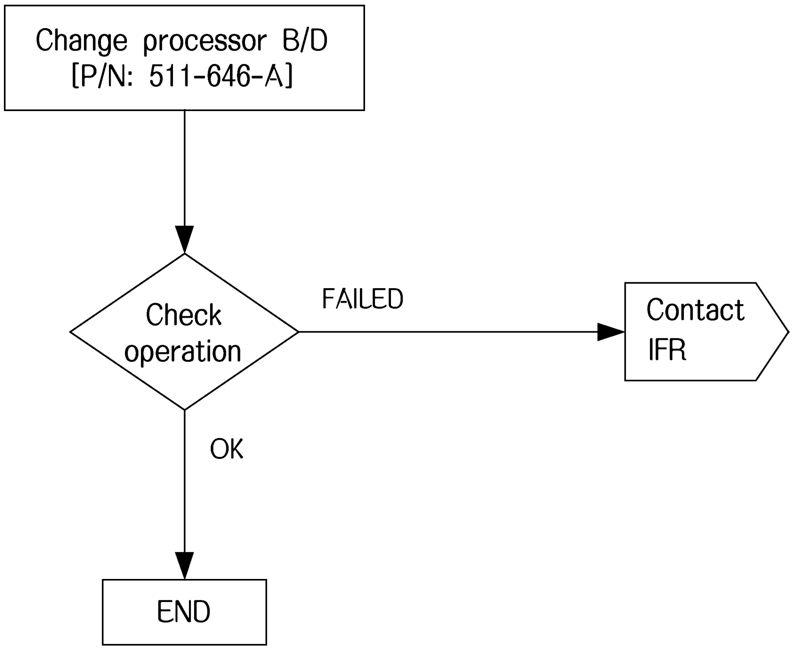

A
Check display of LCD
FAILED
Change inverter assy. [P/N: 511-647-A] (Refer to SECTION 5)
FAILED
OK
OK
OK
Change WH1 [P/N: 550-906-AR1] (Refer to SECTION 5)
FAILED
OK
Change LCD [P/N: 588-066] (Refer to SECTION 5)
FAILED
Contact IFR
Perform power on calibration
B


B
Yig Cal Pass?
NO
YES
Change RF Module [P/N: 7005-2640-500] (Refer to SECTION 5)
Yig Cal Pass?
NO
YES
Change processor B/D assy [P/N: 511-646-A] (Refer to SECTION 5)
Yig Cal Pass?
YES
NO
Contact IFR
Span Cal Pass?
NO
YES
Change processor B/D ass'y [P/N: 511-646-A]
Span Cal Pass?
NO
YES
Contact IFR
Level Cal Pass?
NO
YES
Check output (10.7MHz) of RF module
FAILED
OK
System Condition :
Cal Signal on,CF:40MHz, Ref:-
10.7MHz, level : -30dBm±3dB
on connector WH5 of RF Module
Change RF module [P/N:7005-2640-500]
Level Cal Pass?
NO
YES
Change IF filter B/D [P/N:511-649-A] (Refer to SECTION 5)
NO
Check output level of IF filter B/D
YES
For IF filter B/D output (10.7MHz) (Refer to Note 1)
YES
Level Cal Pass?
NO
Check video output level
OK
FAILED
Refer to Note 2
YES
Level Cal Pass?
Change video B/D [P/N: 511-648-A or 511-706-A QP option] (Refer to SECTION 5)
NO
Change processor B/D assy. [P/N: 511-646-A]
C
D
Note 1
Cal Signal on,CF:40MHz,Ref:-
Output level : +2dBm±3dB
RBW:(3M,1M,300K,100K,30K,10K,3K,1K,300Hz
Note 2
Cal Signal on,CF:40MHz,Ref:-
Output level :

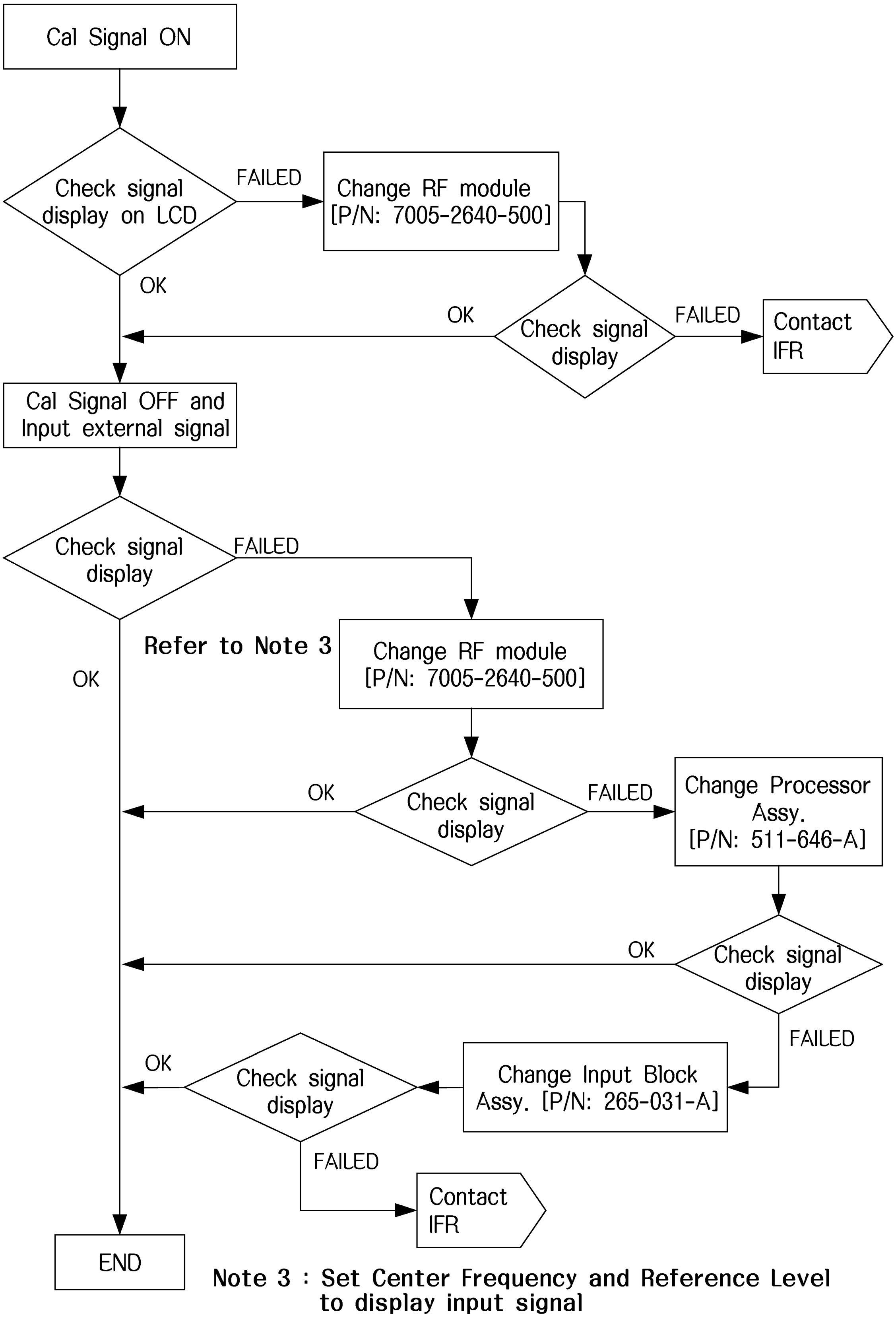

C
D
Level Cal Pass?
YES
NO
Contact IFR
Log Cal Pass?
NO
Check output of video B/D (Refer to Note 2)
FAILED
Change video B/D [P/N: 511-669-A or 511-706-A QP option]
YES
OK
YES
Log Cal Pass?
NO
Change Processor B/D Assy [P/N: 511-646-A]
YES
Log Cal Pass?
NO
Contact IFR
RBW Cal Pass?
NO
Check IF filter B/D assy (Refer to Note 1)
FAILED
Change IF filter B/D assy [P/N:511-649-A]
YES
OK
YES
RBW Cal Pass?
NO
Change processor B/D Ass'y [P/N: 511-646-A]
END
YES
RBW Cal Pass?
NO
Contact IFR

Fault diagnosis procedure for malfunction

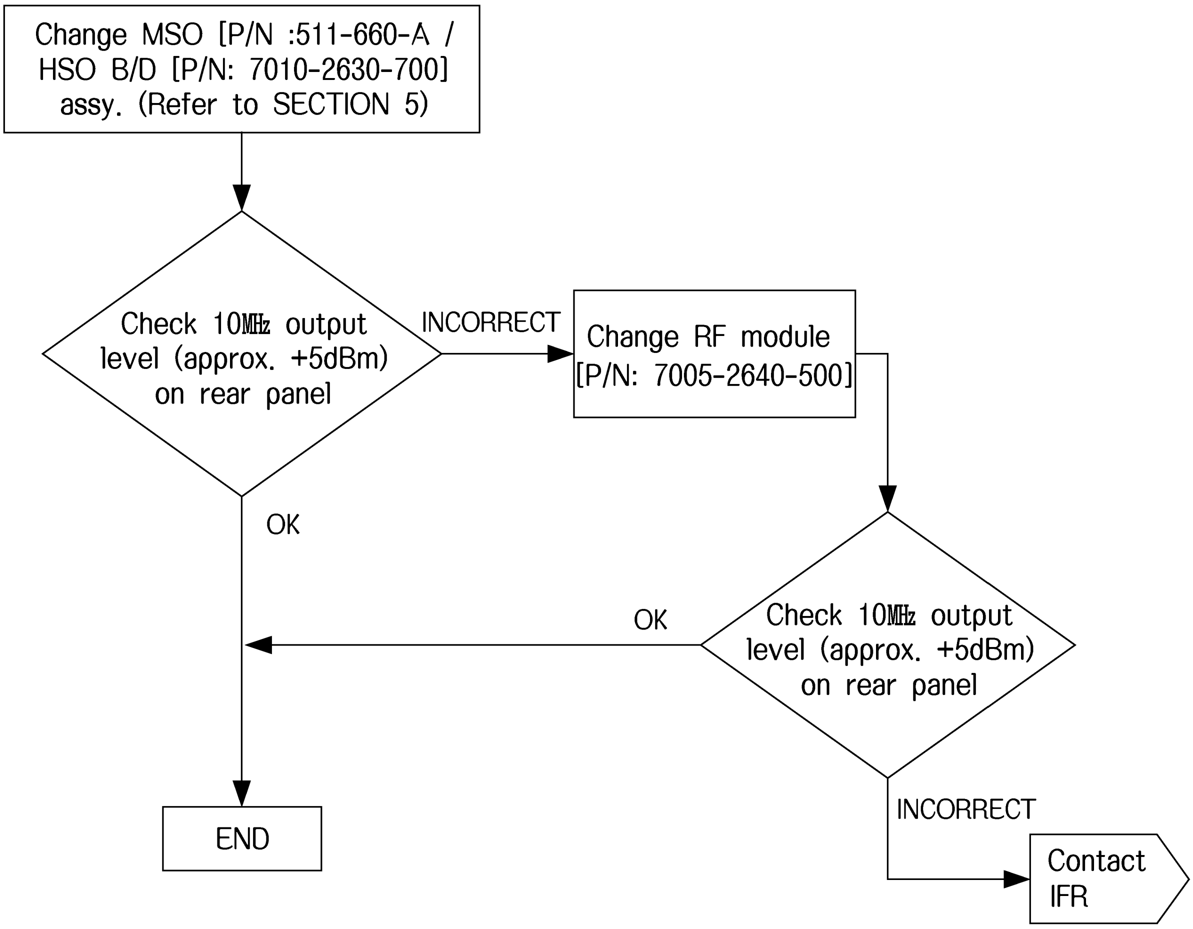
1. Display lock-up after booting



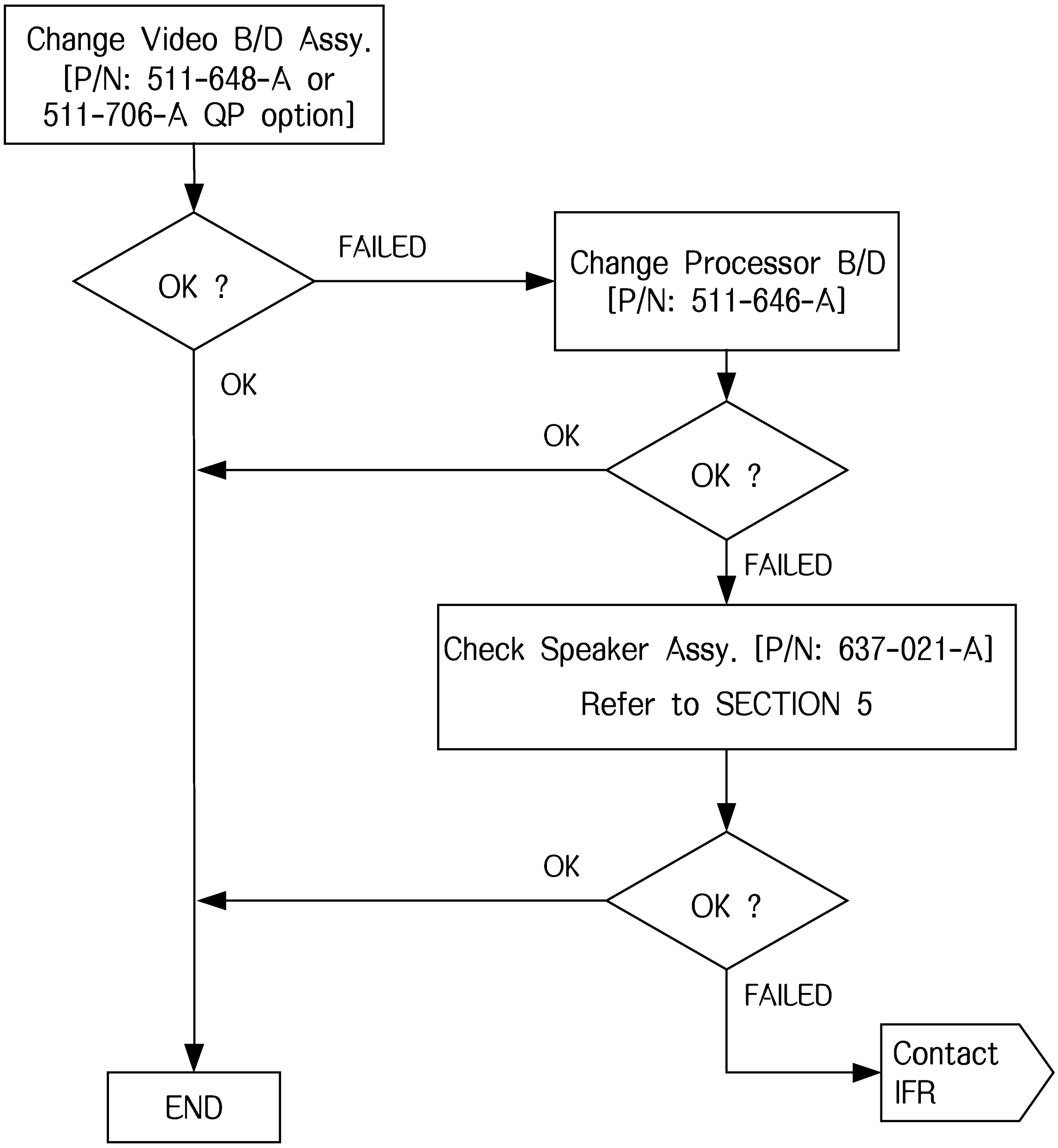
2. No display of RF signal input signal



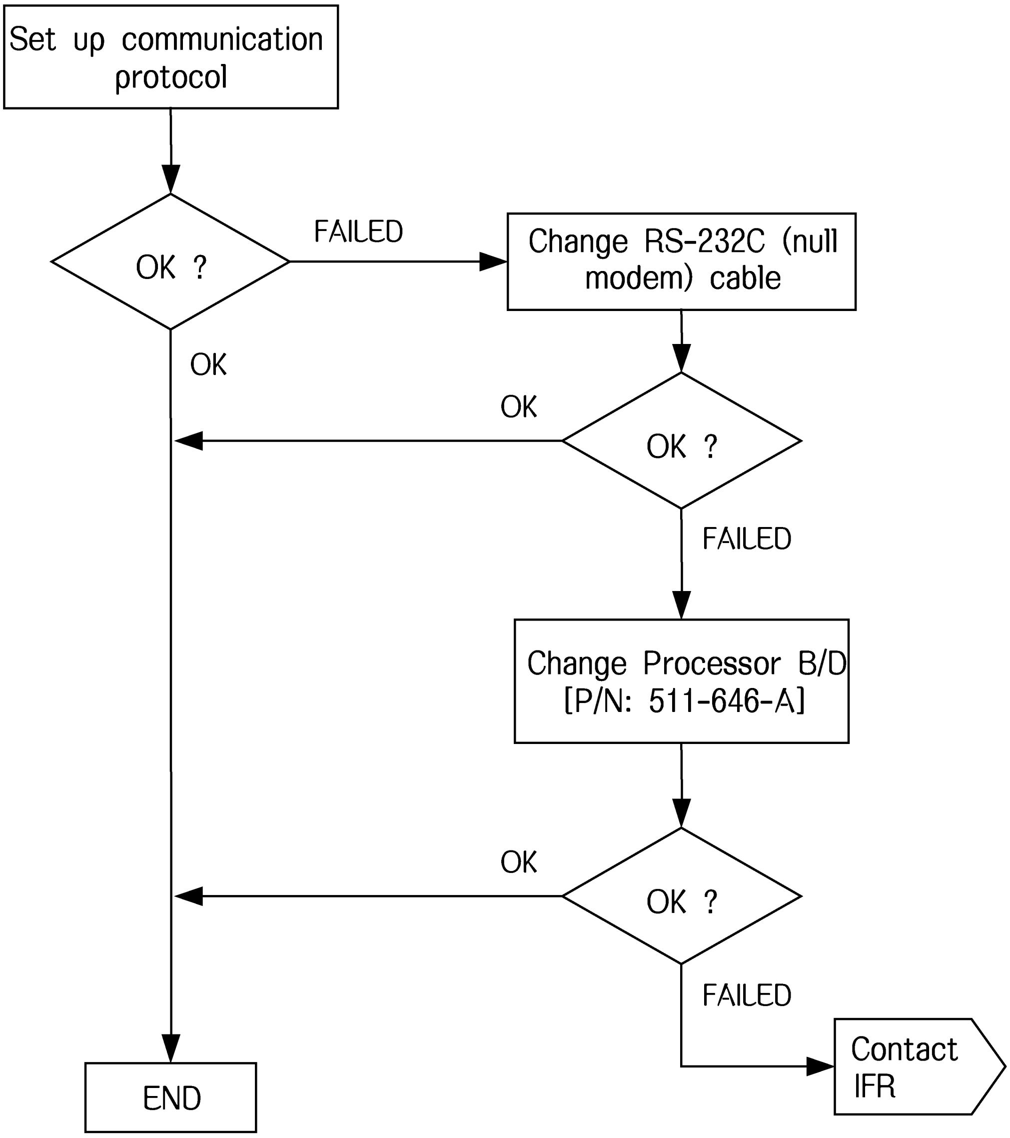
3. No output of 10㎒ reference signal



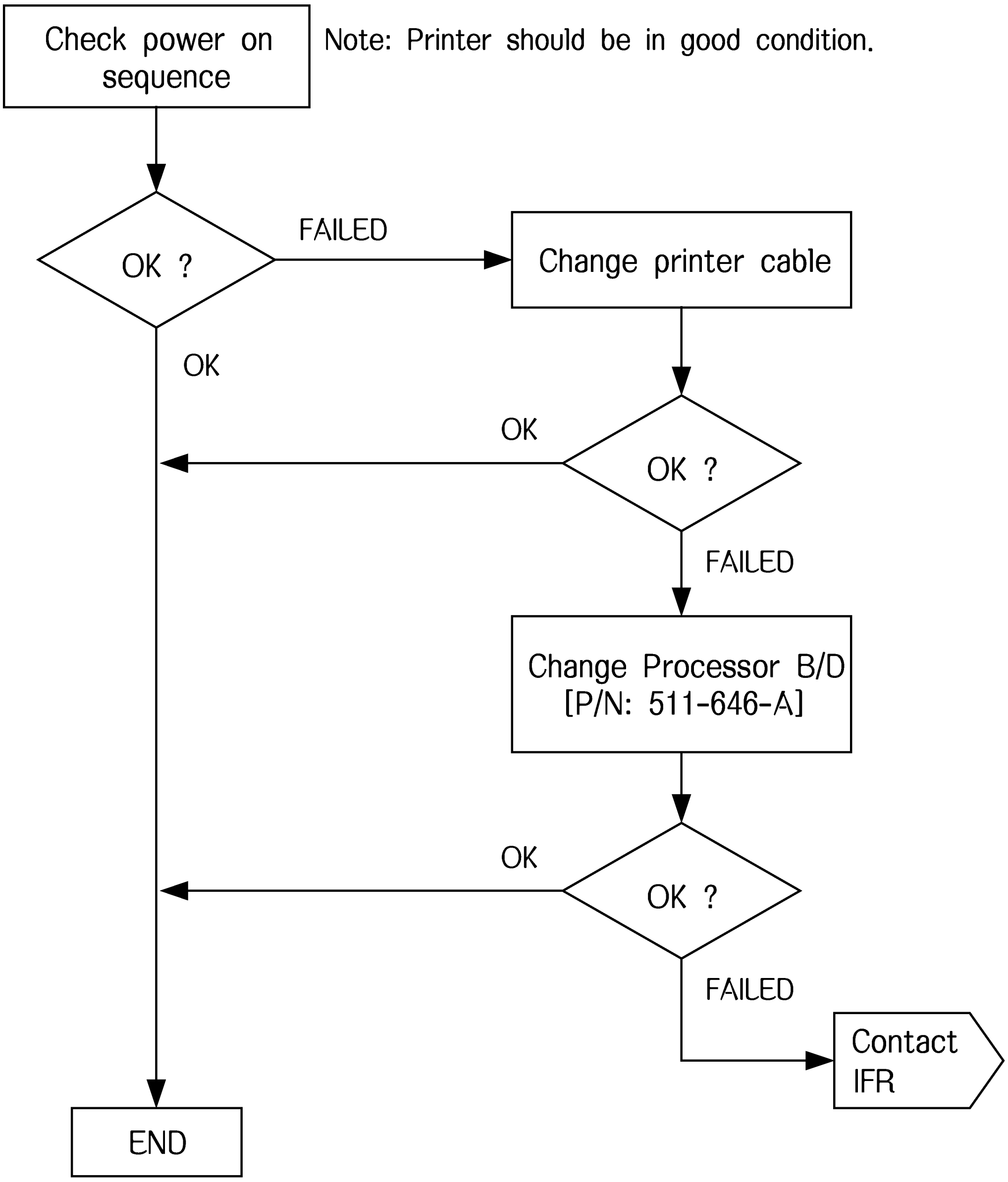
4. No sound on speaker / No output on phone jack



5. RS-232C malfunction (not controllable by computer)

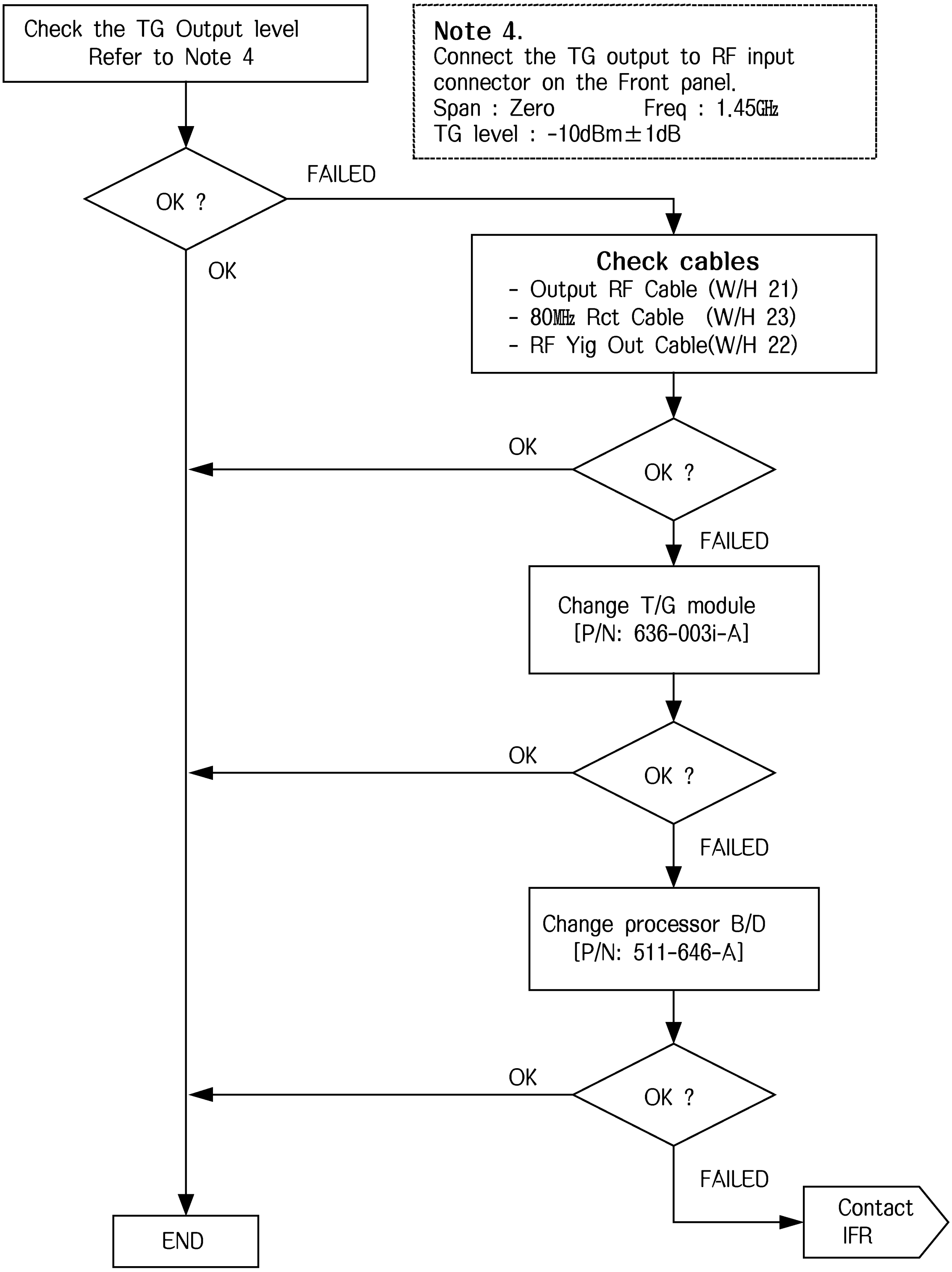


6. Print malfunction



Option malfunction

1. Tracking Generator



Section 5

Replacement Procedures

SECTION 5
REPLACEMENT PROCEDURES

TABLE OF CONTENTS

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SECTION 5
REPLACEMENT PROCEDURES

GENERAL

This section contains instruction for replacement of any assembly contained in the unit. The instructions given are for removal of each assembly. Prerequisite instructions are listed as needed. Reassembly is in reverse order of removal instructions unless otherwise noted. Refer to applicable wiring drawings in Section 6 to verify cable location, if necessary.

CAUTION: TO AVOID DAMAGE WHEN REMOVING A SEMI-RIGID COAXIAL CABLE, LOOSEN THE CONNECTORS AT BOTH ENDS BEFORE FULLY DISCONNECTING AT EITHER END.

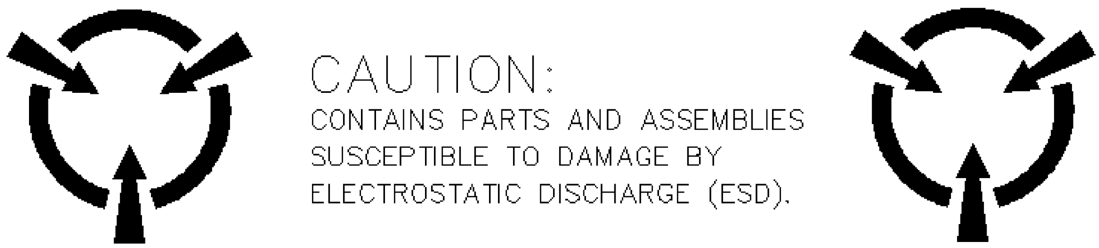
- **SAFETY PRECAUTIONS**

Power should be removed from the unit before any replacement procedure is initiated.

WARNING: DANGEROUS VOLTAGES ARE PRESENT WITH CASE ASSEMBLIES REMOVED IF POWER IS PRESENT.

- **ESD PRECAUTIONS**

CAUTION: THE REPLACEMENT PROCEDURES FOR THE SPECTRUM ANALYZER SHOULD ONLY BE PERFORMED IN AN ESD ENVIRONMENT AND ALL PERSONNEL PERFORMING THE REPLACEMENT PROCEDURES SHOULD HAVE KNOWLEDGE OF ACCEPTED ESD PRACTICES AND/OR BE ESD CERTIFIED.



EQUIPMENT REQUIREMENTS

TOOL	SIZE
SCREWDRIVER	(+) M2, (2~2.5)
SCREWDRIVER	(+) M3, (6~8)
SCREWDRIVER	(+) M4, (10~12)
SCREWDRIVER	(-) 7mm
BOX DRIVER	4mm
BOX DRIVER	5mm
BOX DRIVER	6mm
BOX DRIVER	6.2mm
BOX DRIVER	7mm

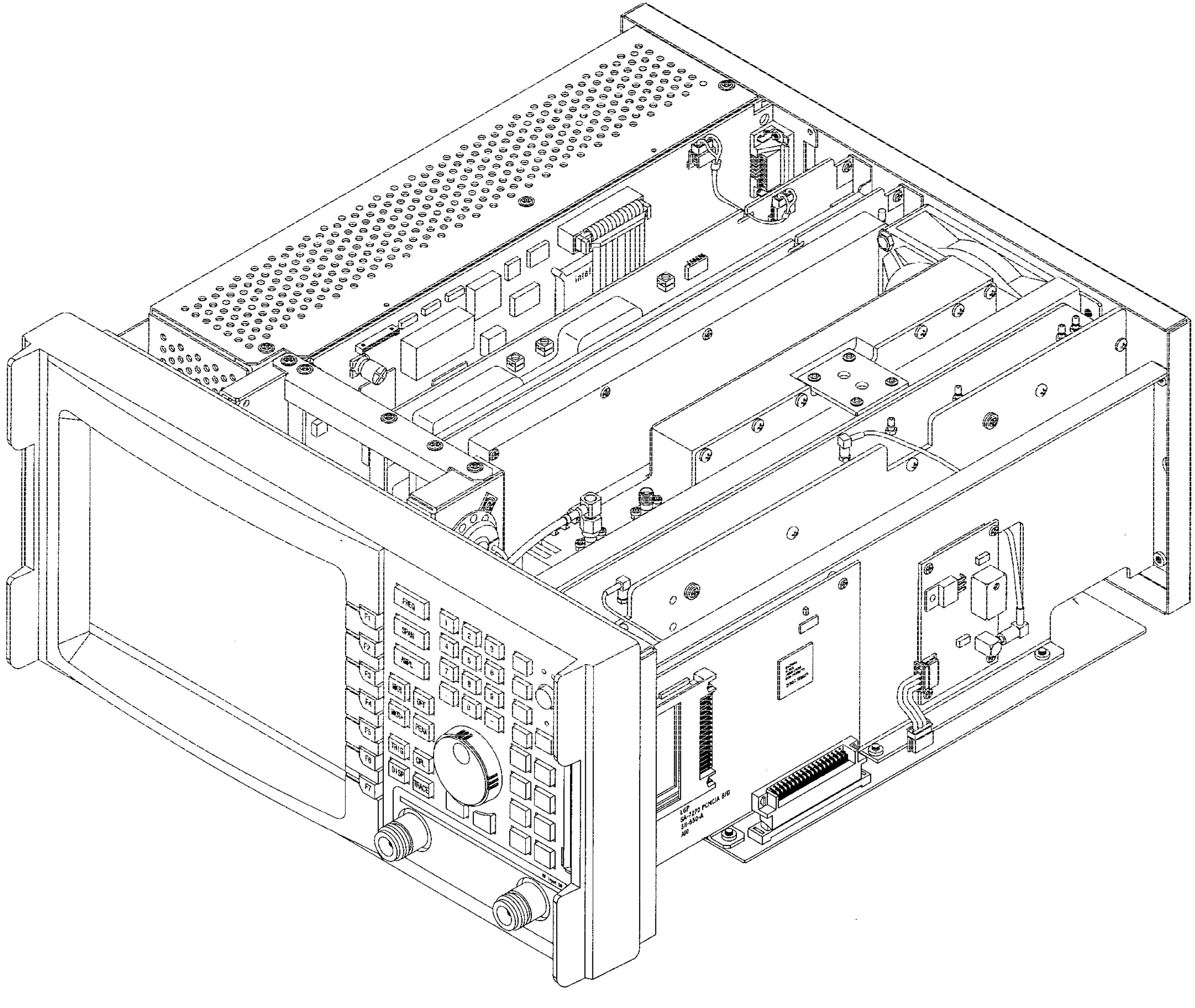


Fig. 5-2-1 FRONT VIEW

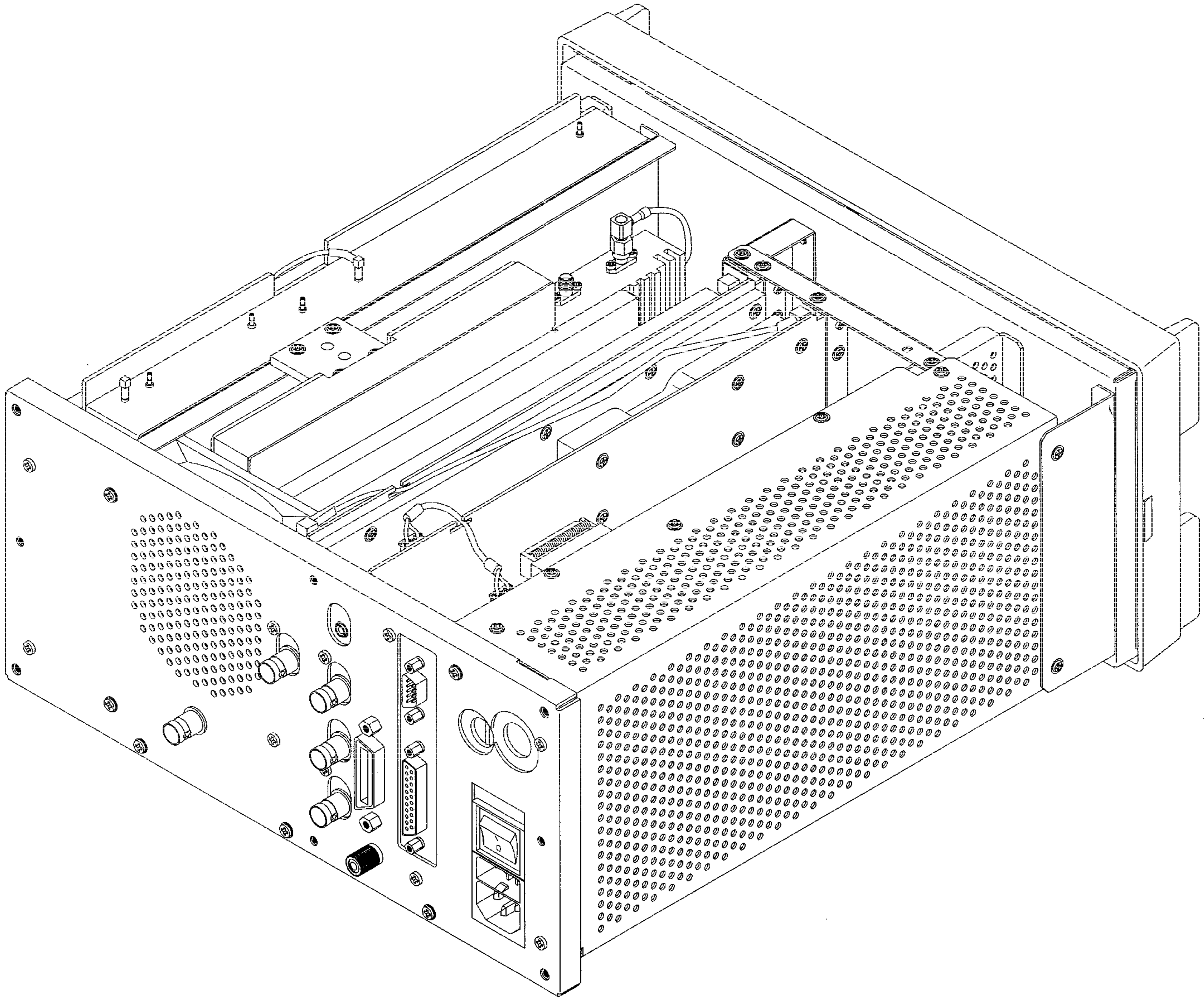


Fig. 5-2-2 REAR VIEW

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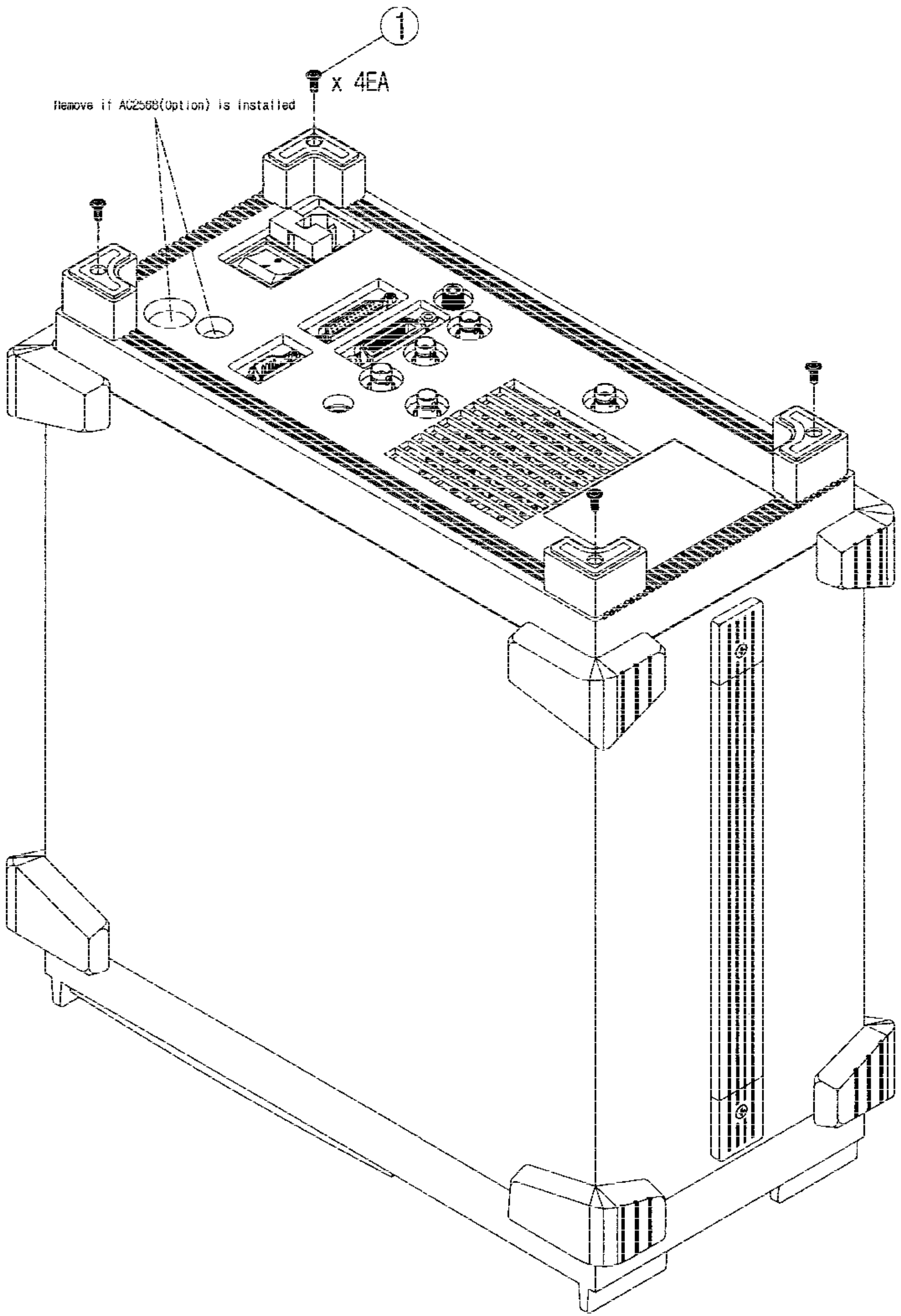

Fig. 5-3-1 REAR PANEL ASSEMBLY
(245-0971-A)

REPLACEMENT PROCEDURES

Rear Panel Assembly

STEP	PROCEDURE
1.	Disconnect AC power.
2.	Set unit (with nothing connected to front panel connector) with front panel face down.
3.	Remove four screws as shown.

Can Cover Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

STEP	PROCEDURE
1.	Remove four screws ①.
2.	Slide Can Cover Assembly ② up and off chassis assembly.

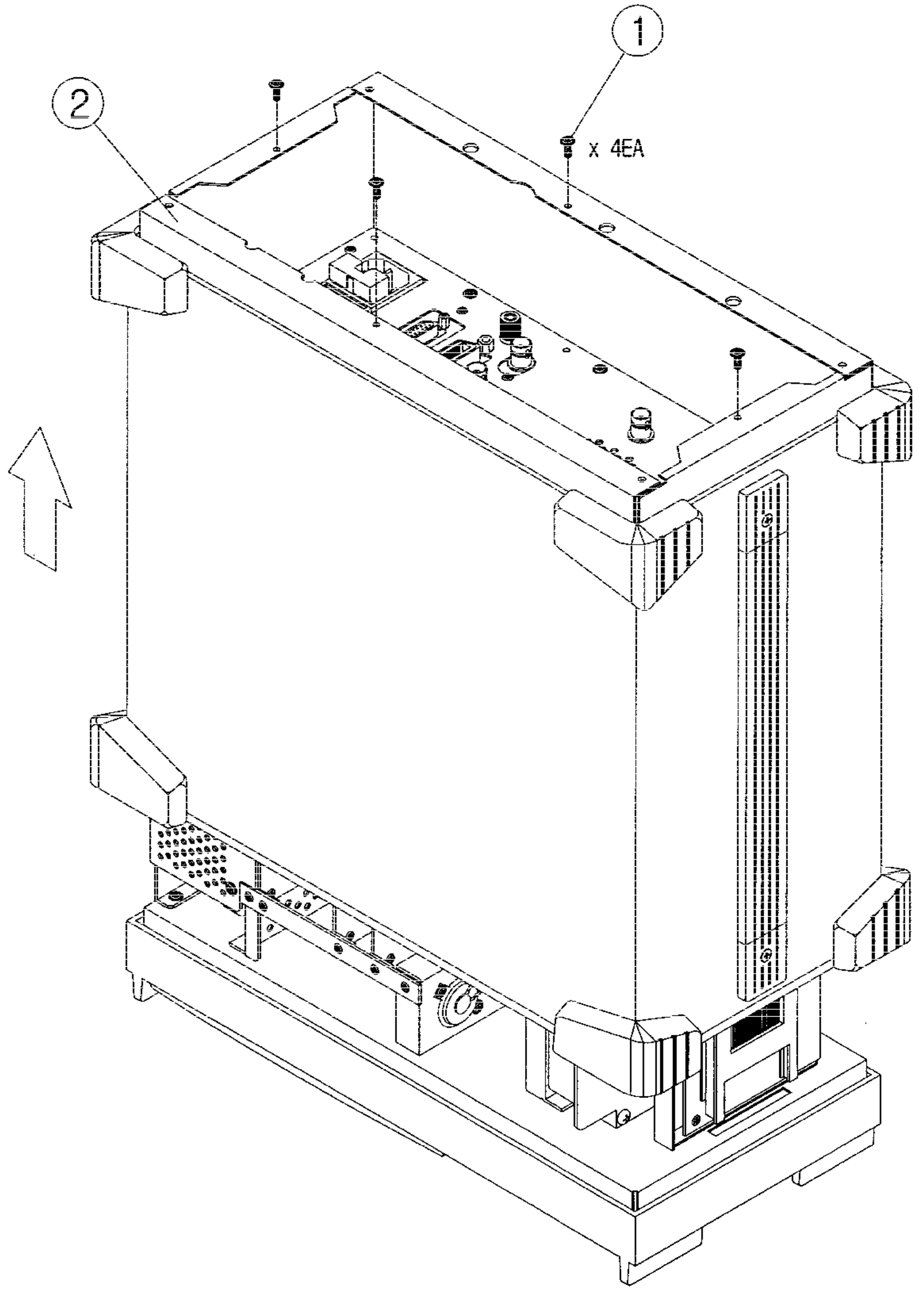

Fig. 5-3-2 CAN COVER ASSEMBLY
(217-1741-A)

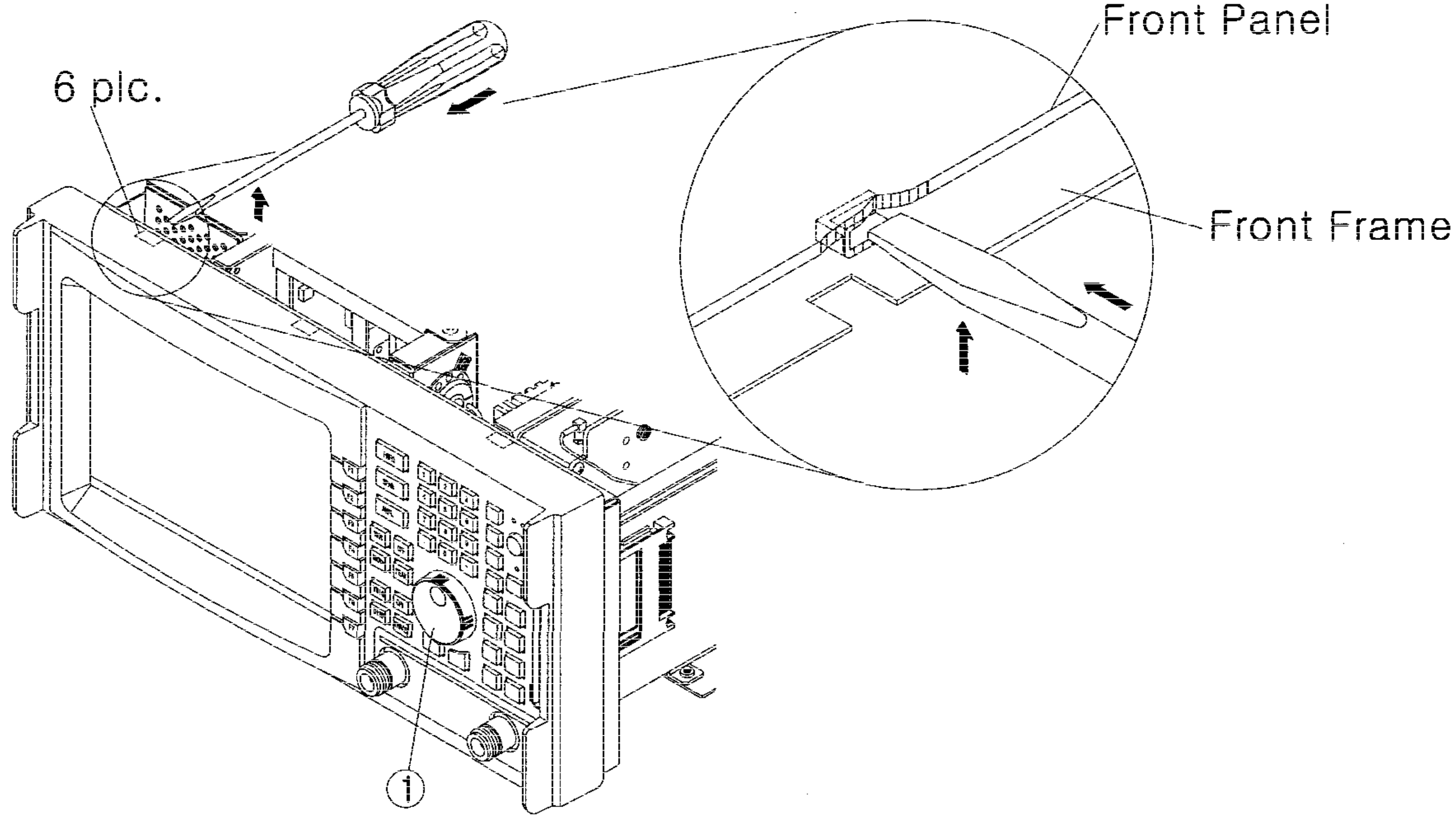

Fig. 5-3-3 FRONT PANEL ASSEMBLY
(245-0961-A)

Front Panel Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove knob ①.
2.	Disengage front panel hooks using a screwdriver (-).
3.	Push front panel up and pull forward.

Front Frame Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

Remove Front Panel Assembly (p. 5-13)

STEP	PROCEDURE
1.	Remove wire harness ①.
2.	Remove 10 screws ②.

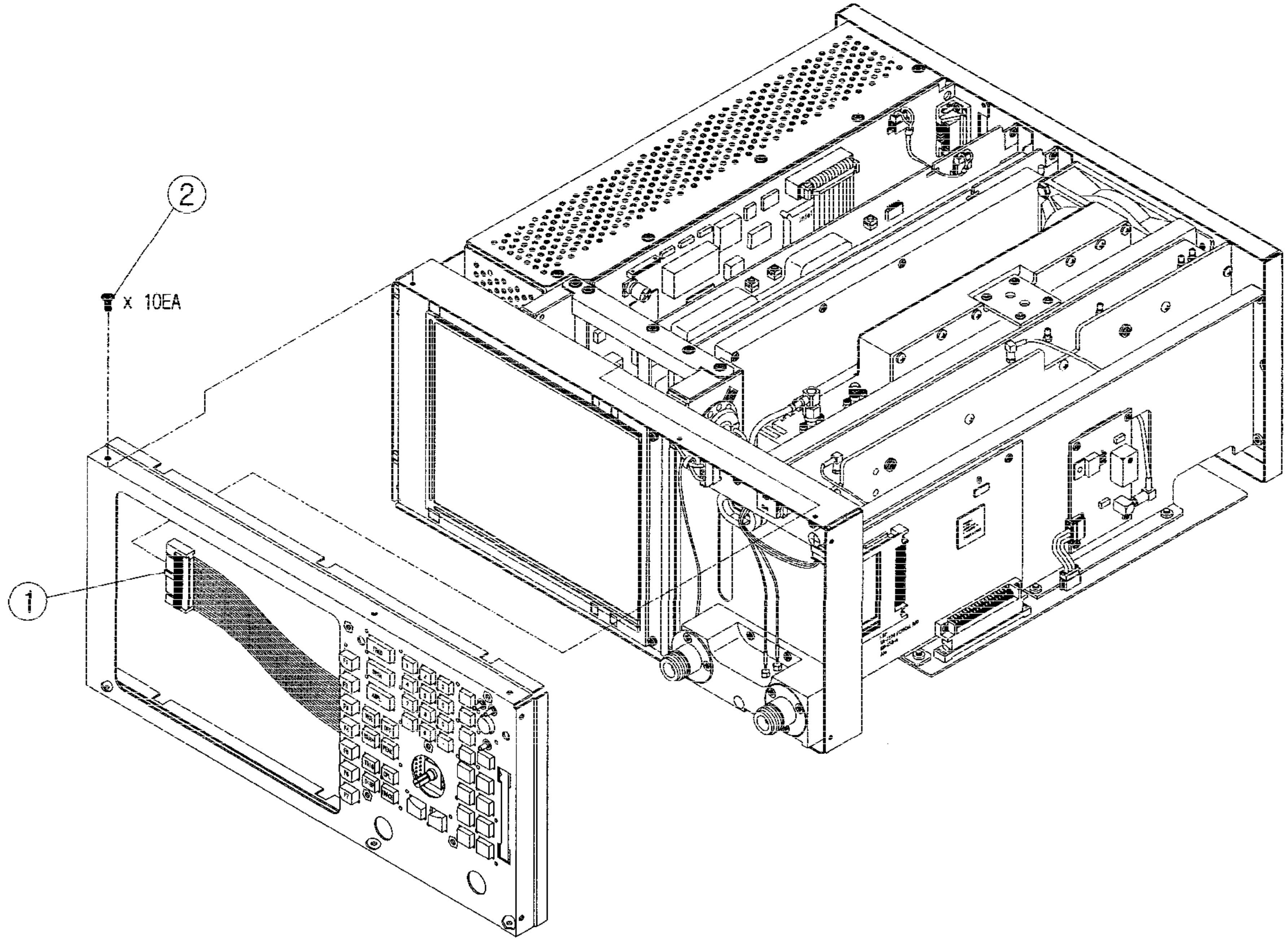

Fig. 5-3-3-1 FRONT FRAME ASSEMBLY
(212-0031-A)

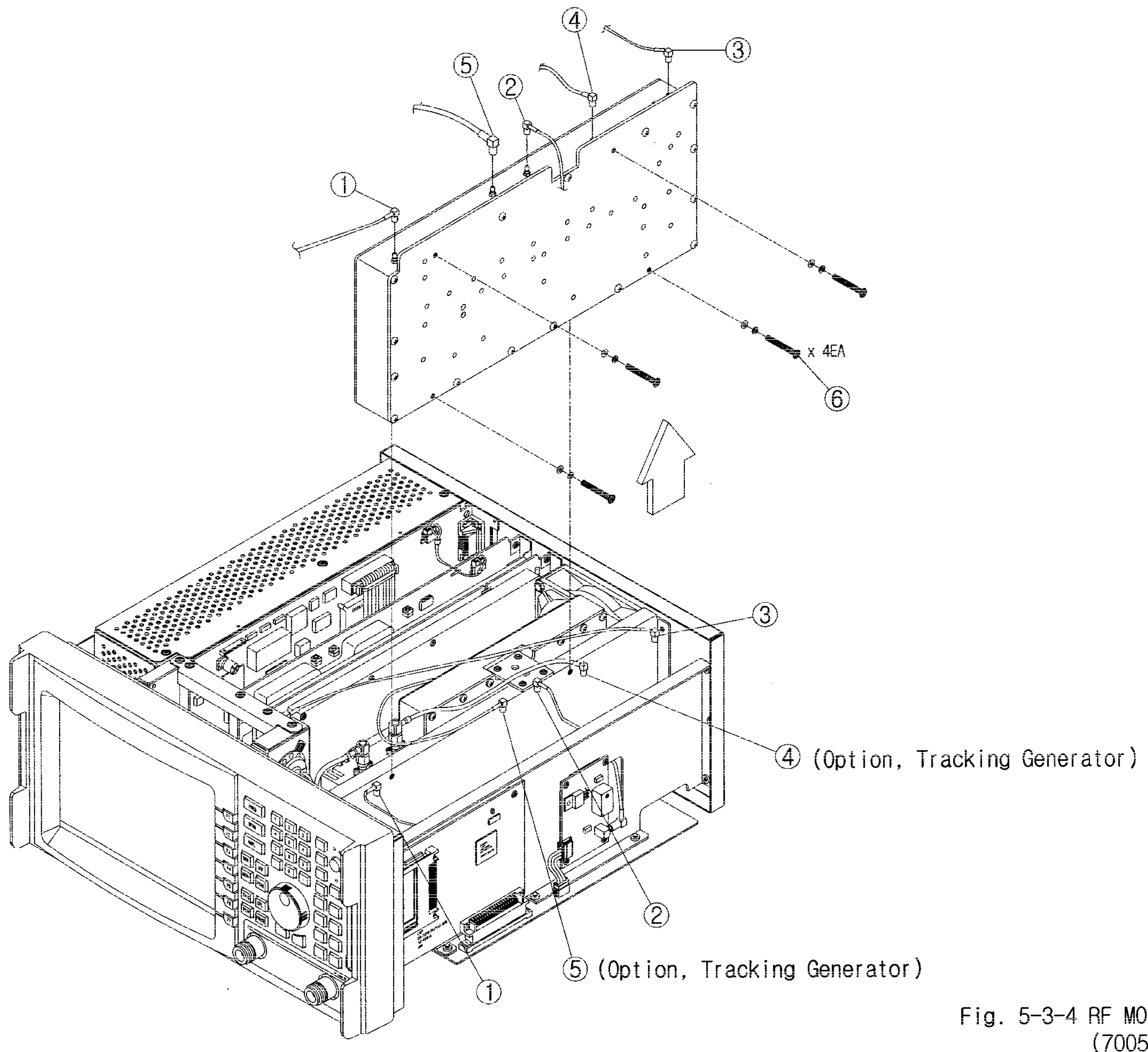

Fig. 5-3-4 RF MODULE ASSEMBLY
(7005-2640-500)

RF Module Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove three connectors ①②③.
	(If Tracking Generator (option) is installed, remove five connectors ①②③④⑤.)
2.	Remove four screws ⑥.
3.	Remove RF Module from the top as shown.

IF Filter and Amp. Board Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP **PROCEDURE**

1. Remove connectors ①.
2. Remove connectors ②.
3. Remove five screws ③ and bracket ⑥.
4. Turn the 2398 over and remove screw ④.
5. Remove two screws ⑤ from the bottom of the 2398.
6. Remove the assembly from the top as shown.

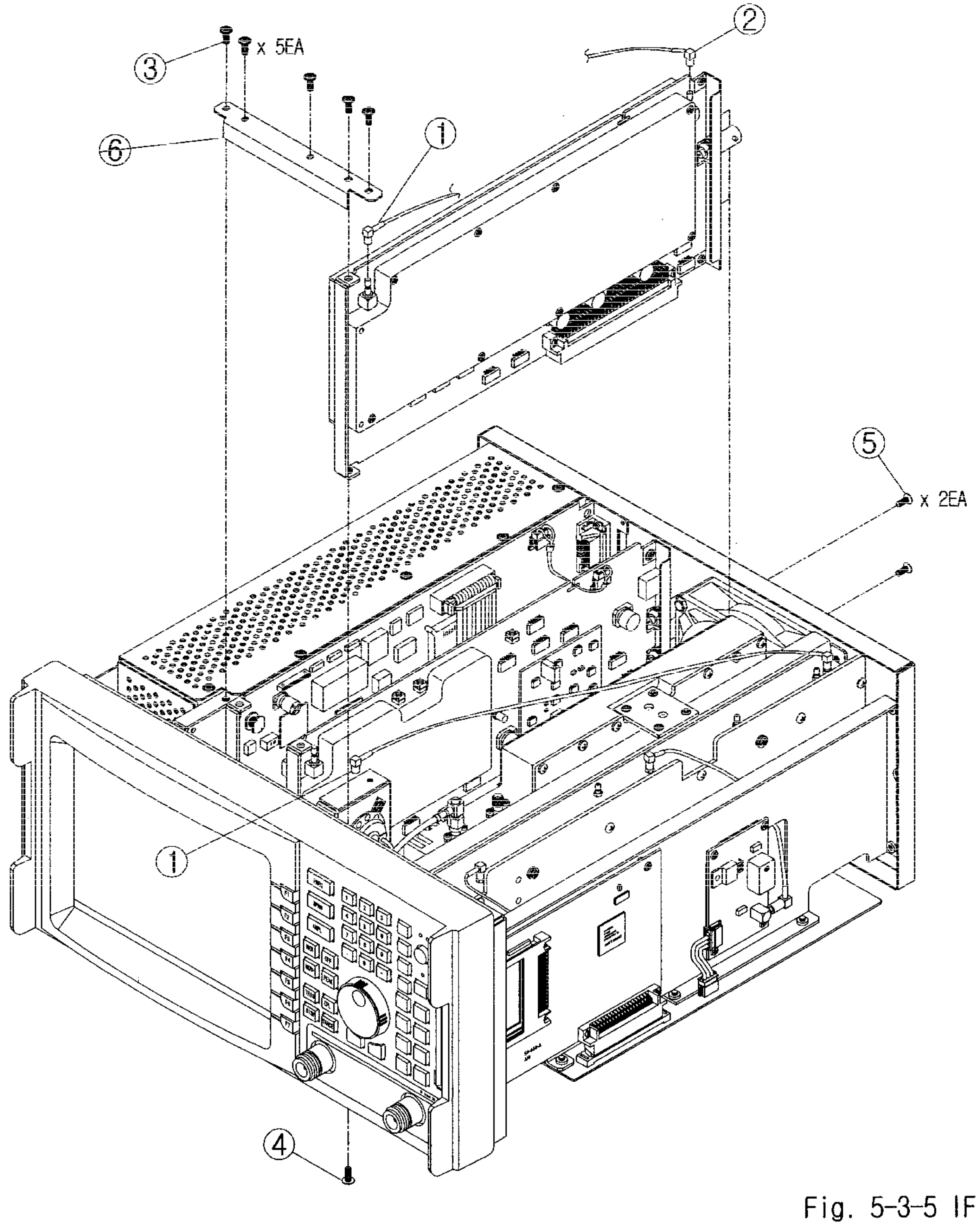

Fig. 5-3-5 IF FILTER AND AMP BOARD ASSEMBLY
(511-649-A)

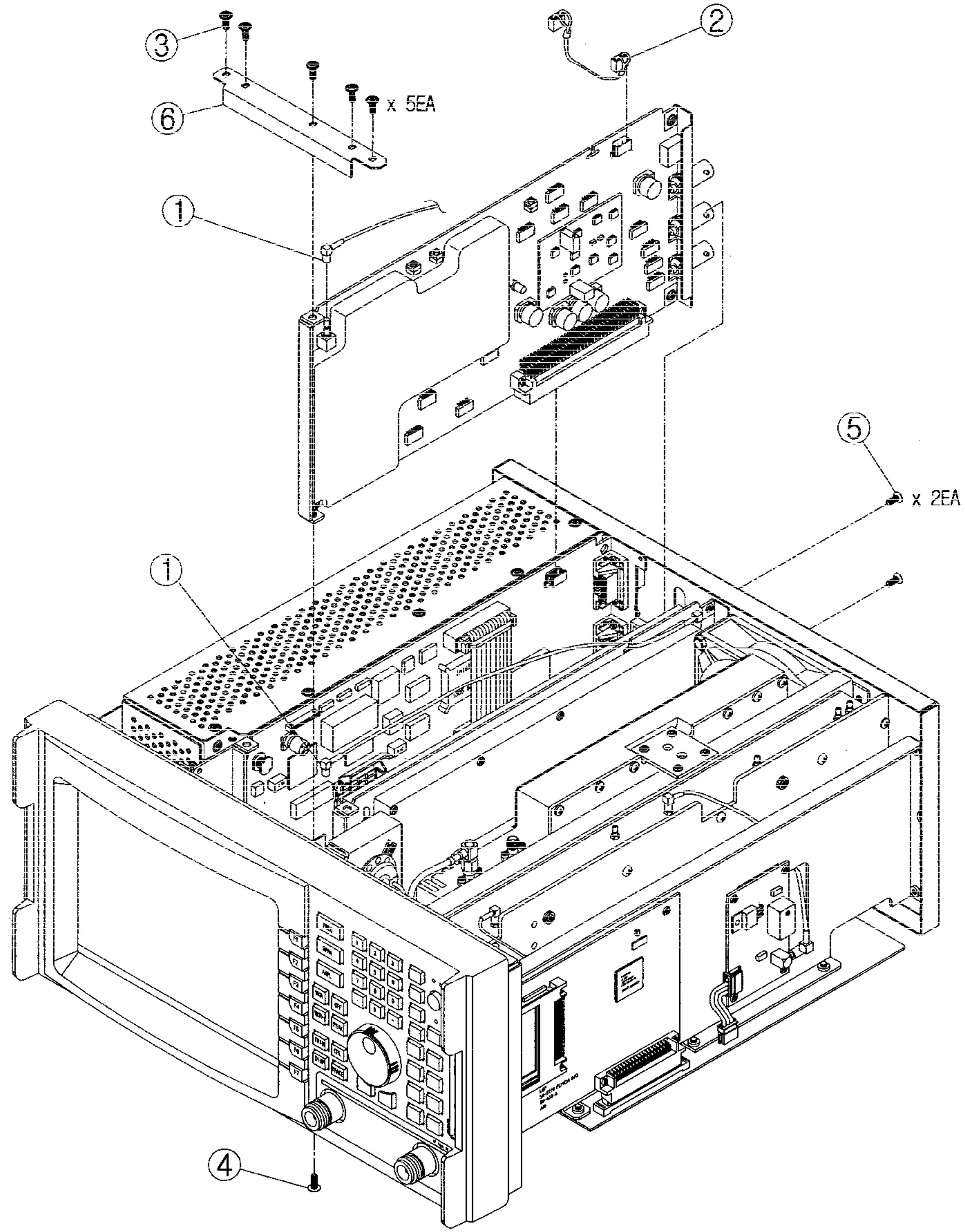

Fig. 5-3-6 VIDEO DETECTOR BOARD ASSEMBLY
(511-648-A)

Video Detector Board Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove connector ①.
2.	Remove wire harness ②.
3.	Remove five screws ③.
4.	Turn the 2398 turn over and remove screw ④.
5.	Remove two screws on the bottom of the 2398 ⑤.
6.	Remove the assembly from the top as shown.

Processor Board Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove wire harness ① (which connects to Video Assembly).
2.	Remove wire harness ② (which connects to LCD Module).
	(If GPIB is installed, remove wire harness ③.)
3.	Remove five screws ④ and bracket ⑧.
4.	Remove wire harness ⑤ (which connects to keyboard).
5.	Turn the 2398 over and remove screws ⑥.
6.	Remove two screws ⑦ from the bottom of the 2398.
7.	Remove the assembly from the top as shown.

(CAUTION! When removing Processor assembly, keep the assembly from touching the Video assembly to prevent damage to the Processor assembly surface mount (solder side) devices.

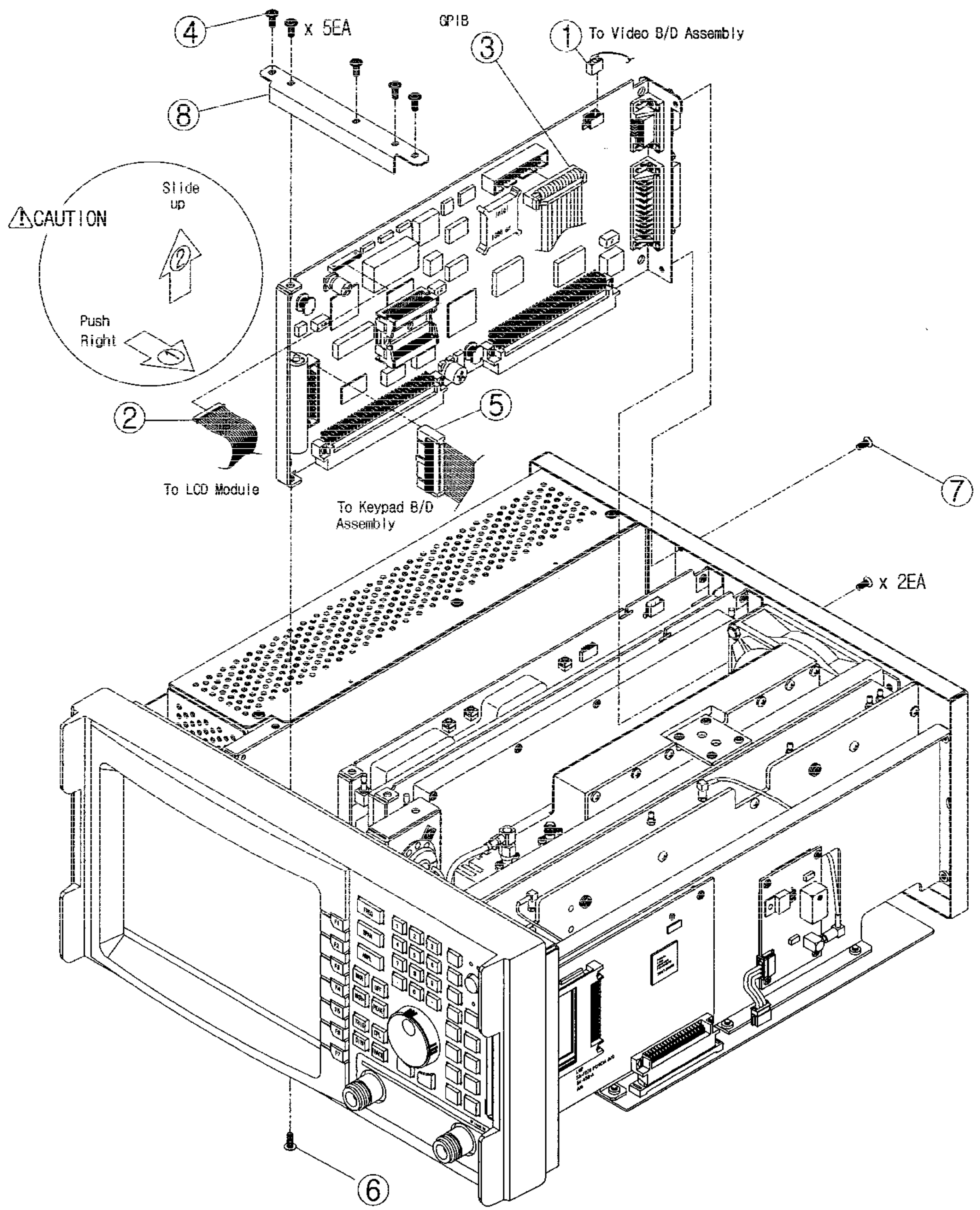

Fig. 5-3-7 PROCESSOR BOARD ASSEMBLY
(511-646-A)

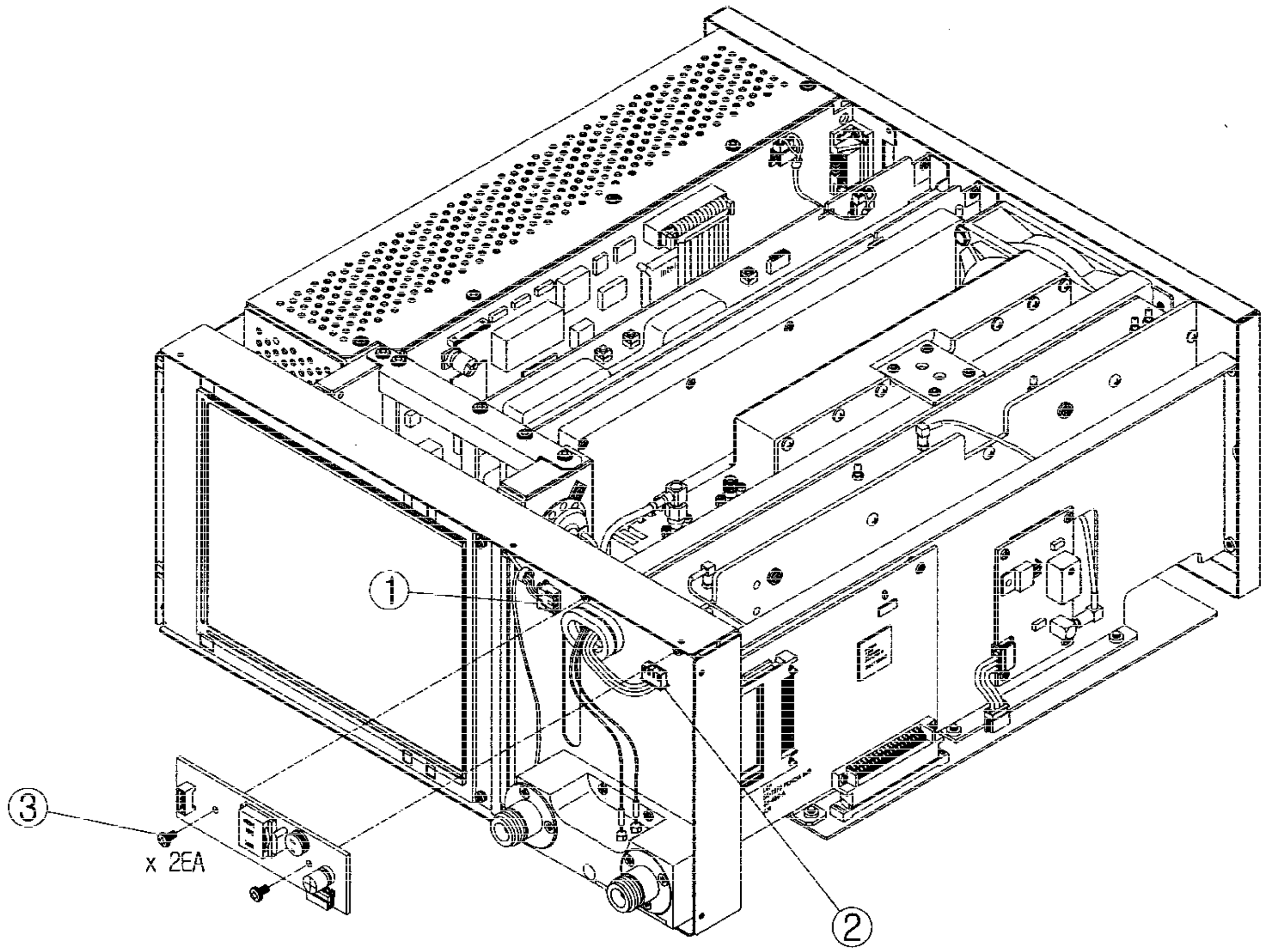

Fig. 5-3-8 LCD INVERTER BOARD ASSEMBLY
(511-647-A)

LCD Inverter Board Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

Remove Front Panel Assembly (p. 5-13)

Remove Front Frame Assembly (p. 5-14)

STEP	PROCEDURE
1.	Remove wire harnesses ① (which connects to LCD Module).
2.	Remove wire harnesses ② (which connects to Motherboard Assembly).
3.	Remove two screws ③.
4.	Remove assembly as shown.

Keyboard Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

Remove Front Panel Assembly (p. 5-13)

Remove Front Frame Assembly (p. 5-14)

STEP	PROCEDURE
1.	Remove five screws from inside of front frame ①.
2.	Remove Keyboard Assembly ②.
3.	Separate keypad ③ from Keyboard Assembly.

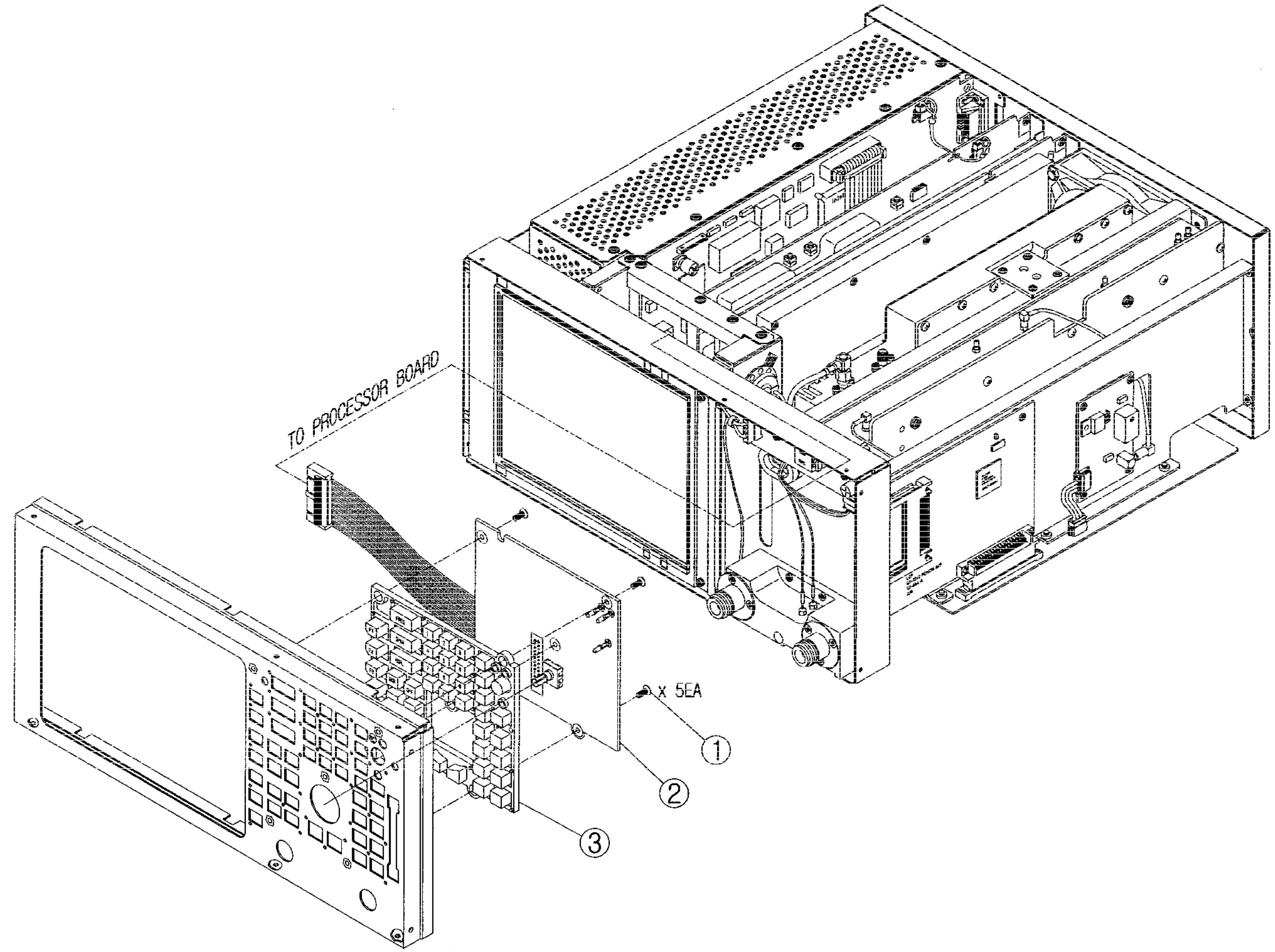

Fig. 5-3-9 KEYPAD BOARD ASSEMBLY
(511-643-A)

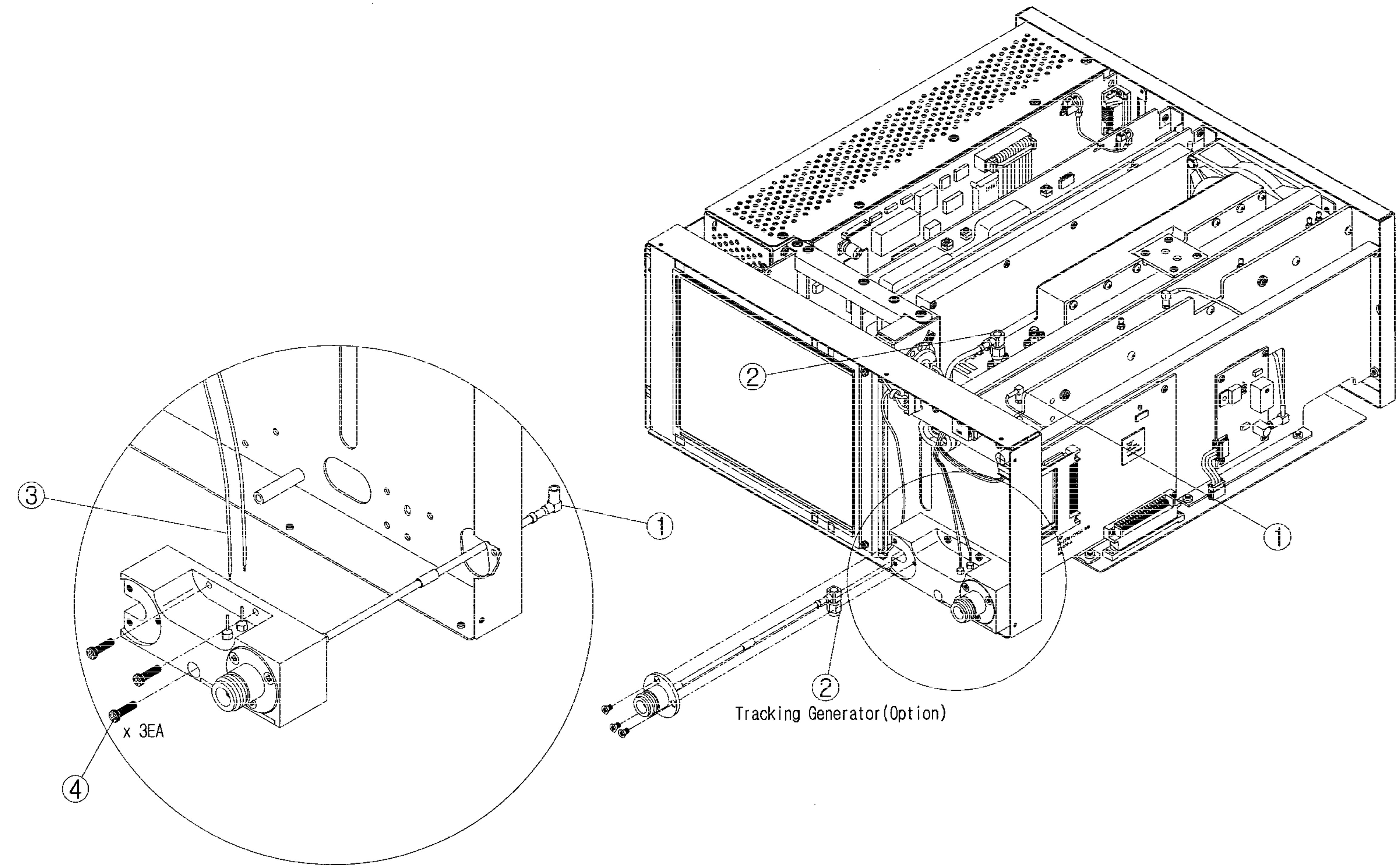

Fig. 5-3-10 RF INPUT BLOCK ASSEMBLY
(265-031-A)

RF Input Block Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

Remove Front Panel Assembly (p. 5-13)

Remove Front Frame Assembly (p. 5-14)

STEP	PROCEDURE
1.	Remove Connector ①. (If Tracking Generator (option) is installed, remove connector ②.)
2.	Remove two parts of wire harness ③ (which connect to feed-thrus.)
3.	Remove three screws ④.
4.	Remove assembly from the front as shown.

MSO / (HSO Option) Board Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove connector ①.
2.	Remove wire harness ②.
3.	Remove four screws ③
4.	Remove assembly from the side as shown.

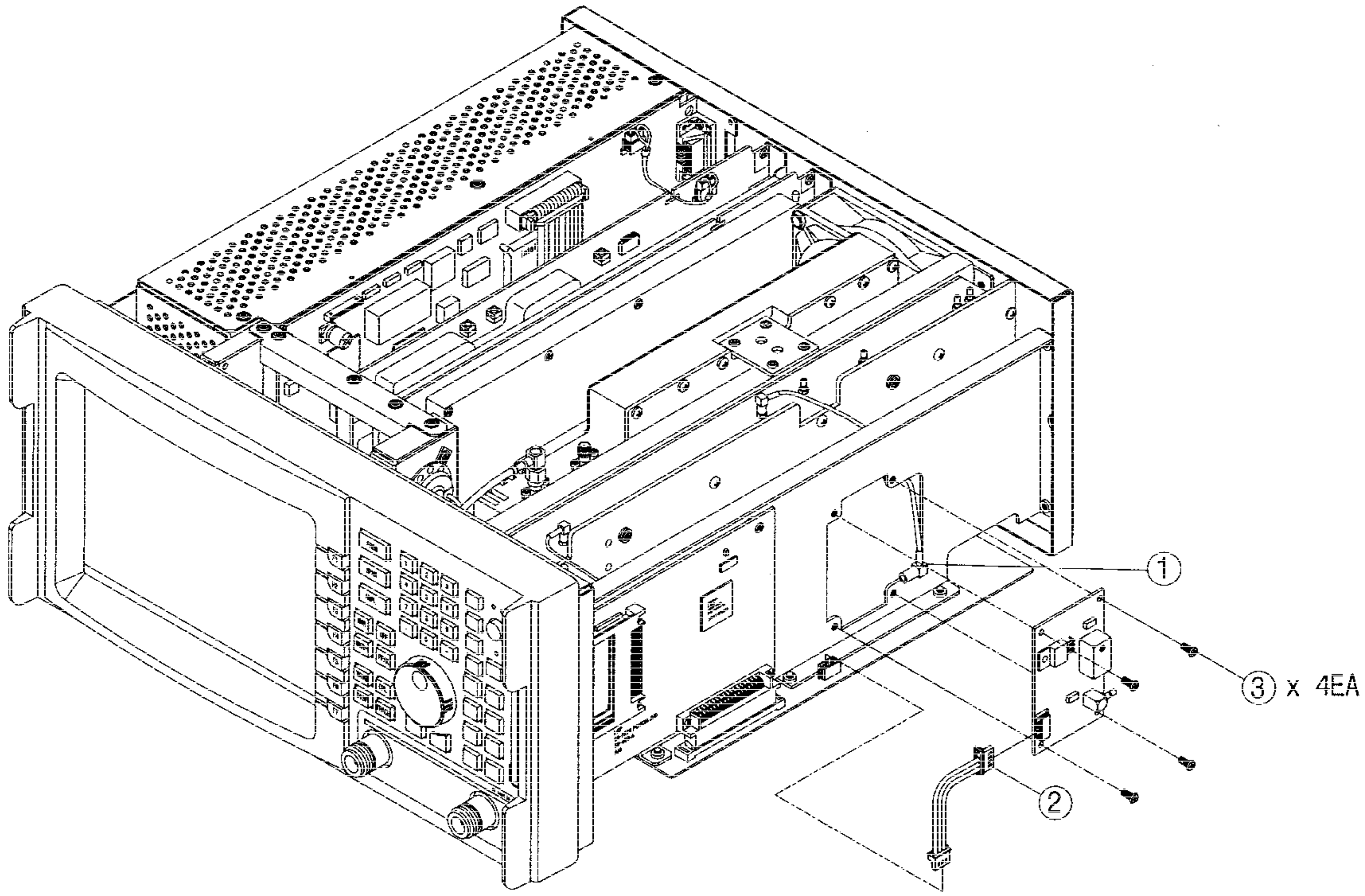

Fig. 5-3-11 MSO/HSO BOARD (OPTION) ASSEMBLY
(511-660-A / 7010-2630-700)

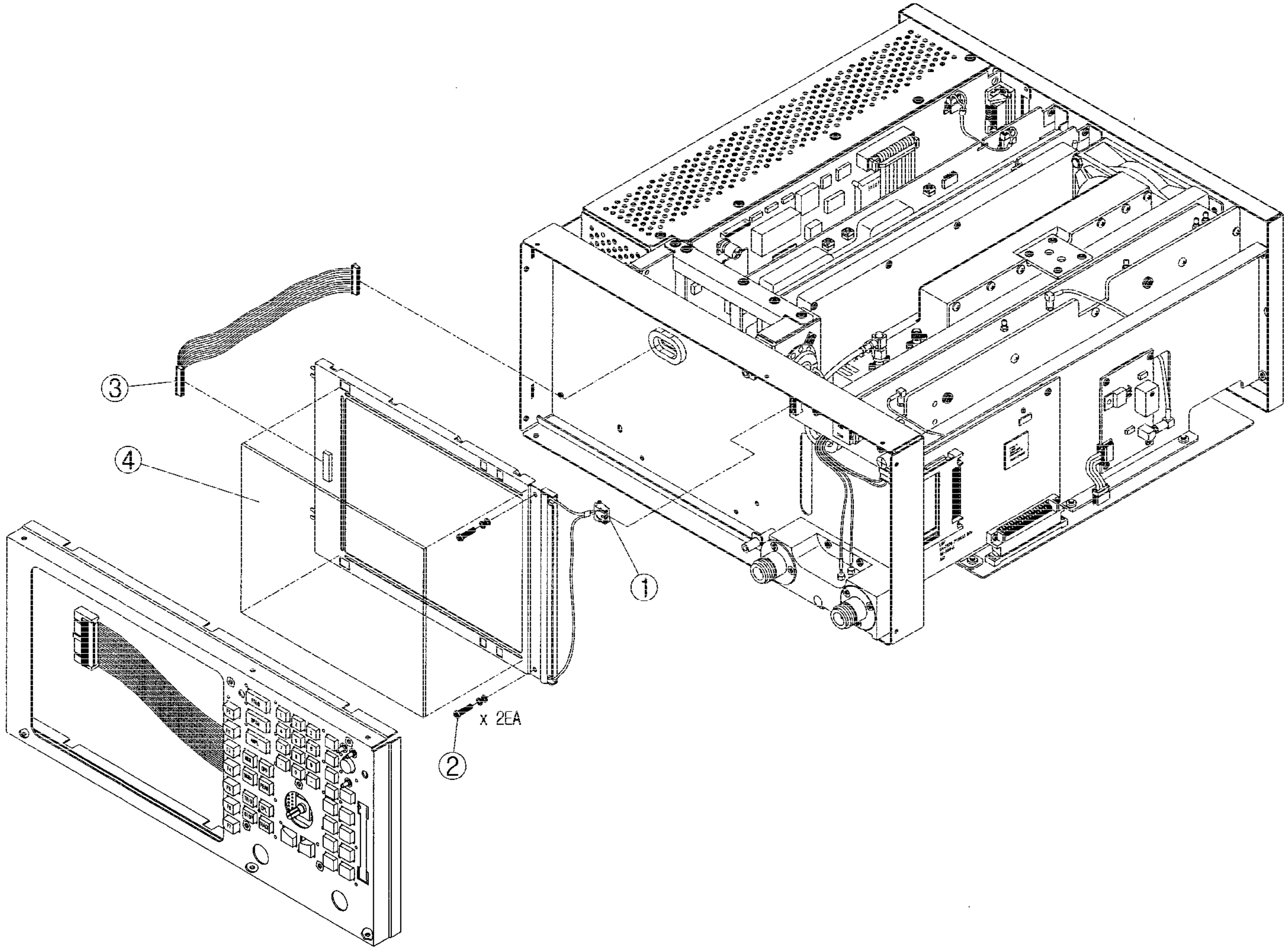

Fig. 5-3-12 LCD FRAME ASSEMBLY
(588-066-A)

LCD Module Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

Remove Front Panel Assembly (p. 5-13)

Remove Front Frame Assembly (p. 5-14)

STEP	PROCEDURE
1.	Remove wire harness ① (which connects to LCD inverter board assembly).
2.	Remove two screws ②.
3.	Remove LCD Module and remove wire harness ③.
4.	Remove LCD window ④.

AC Power Supply Module Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove two screws ①.
2.	Remove four screws ② on side.
3.	Remove two screws ③ from the bottom of the 2398.
4.	Remove the assembly from the top as shown.

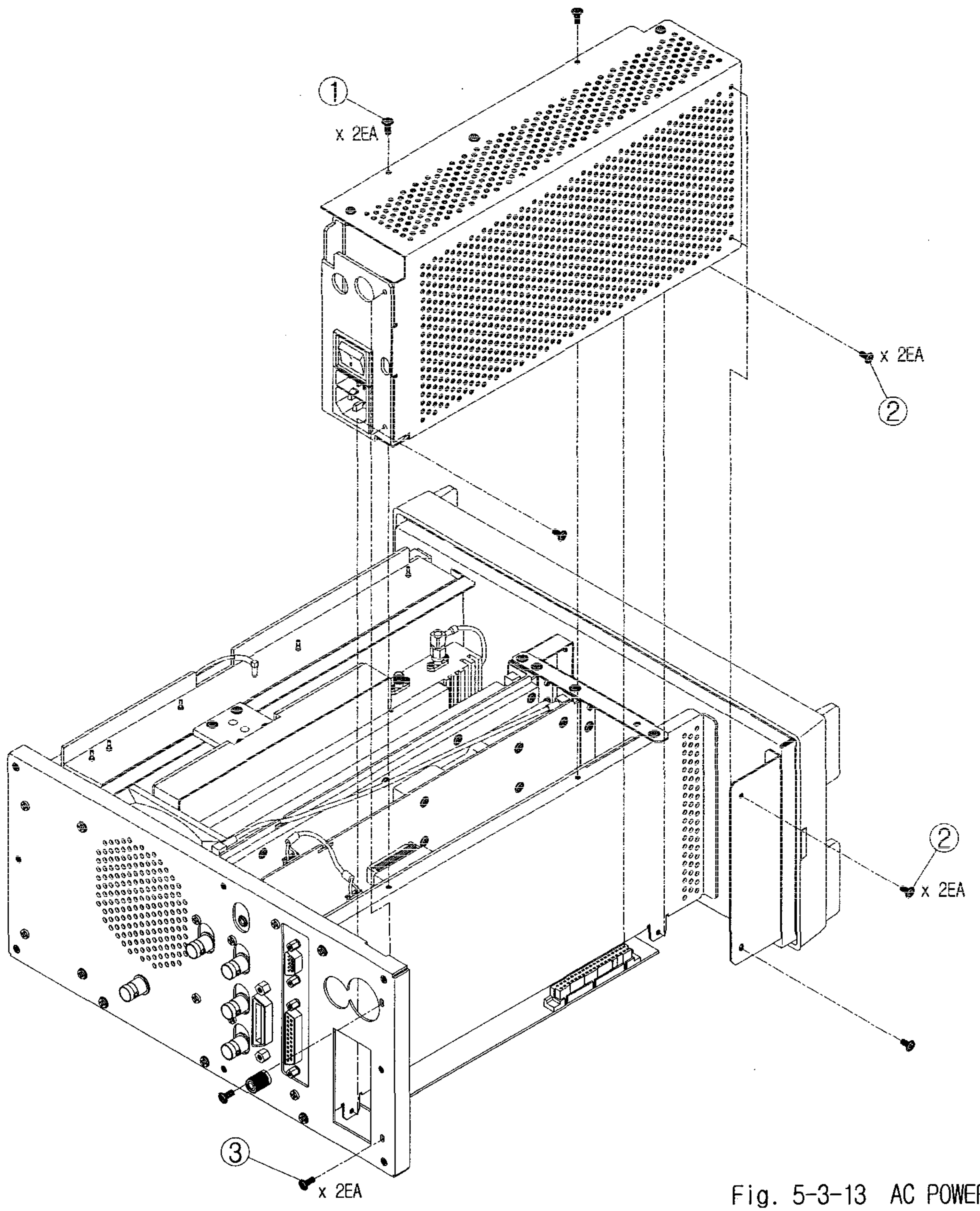

Fig. 5-3-13 AC POWER SUPPLY MODULE ASSEMBLY
(516-003-A)

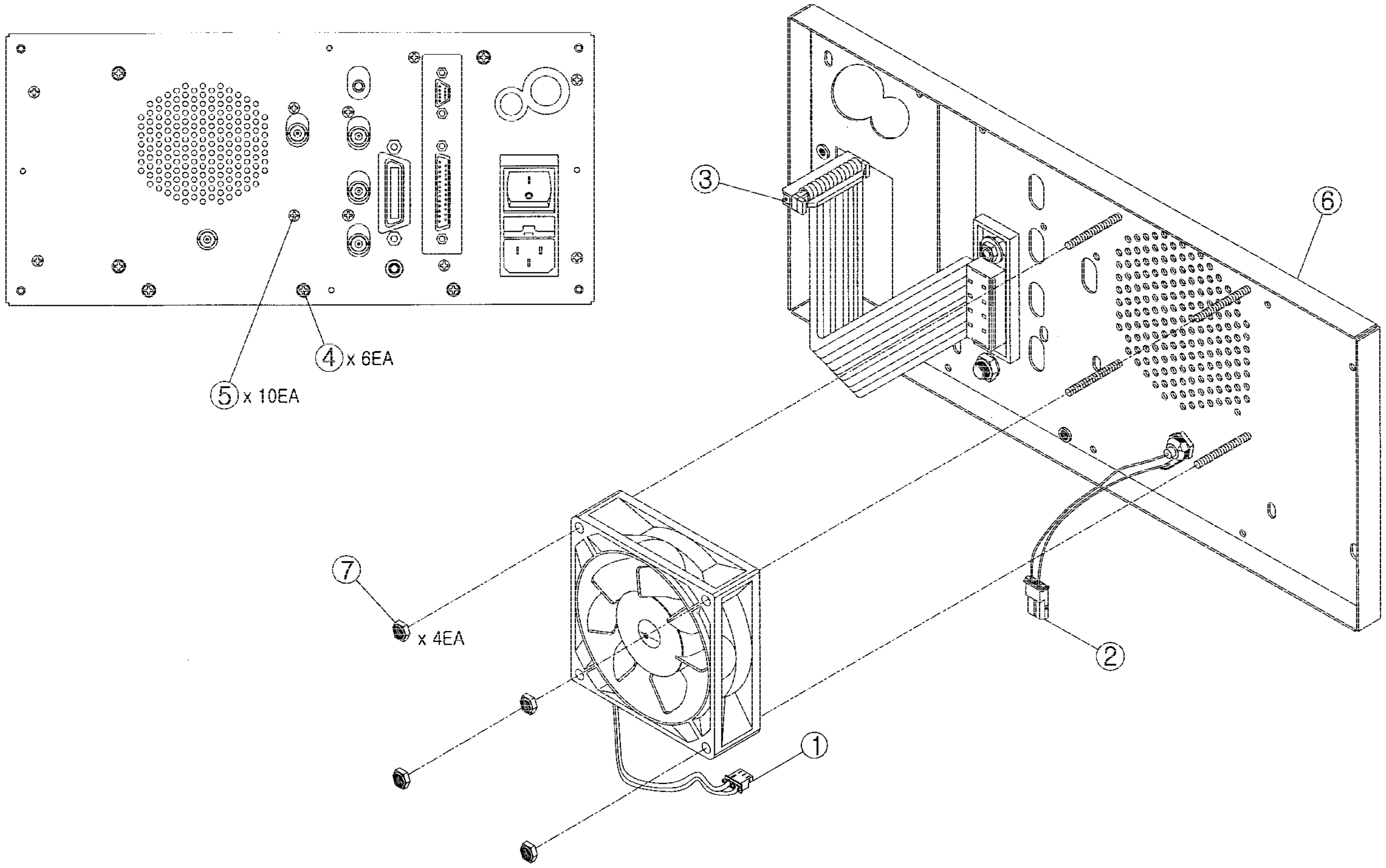

Fig. 5-3-14 DC FAN ASSEMBLY
(639-010-A)

DC Fan Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP **PROCEDURE**

1. Remove wire harnesses ① ② ③.
2. With the 2398 stood on its front panel, remove six screws ④ and ten screws ⑤.
3. Remove rear frame assembly ⑥.
4. Remove four nuts ⑦.
5. Remove the assembly as shown.

Speaker Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

Remove Front Panel Assembly (p. 5-13)

Remove Front Frame Assembly (p. 5-14)

Remove LCD Module Assembly (p. 5-33)

STEP	PROCEDURE
1.	Remove wire harness ①.
2.	Remove five screws ② and bracket ⑥.
3.	Remove two screws ③.
4.	Remove PCB support bracket ④.
5.	Remove two screws ⑤.
6.	Remove the assembly as shown.

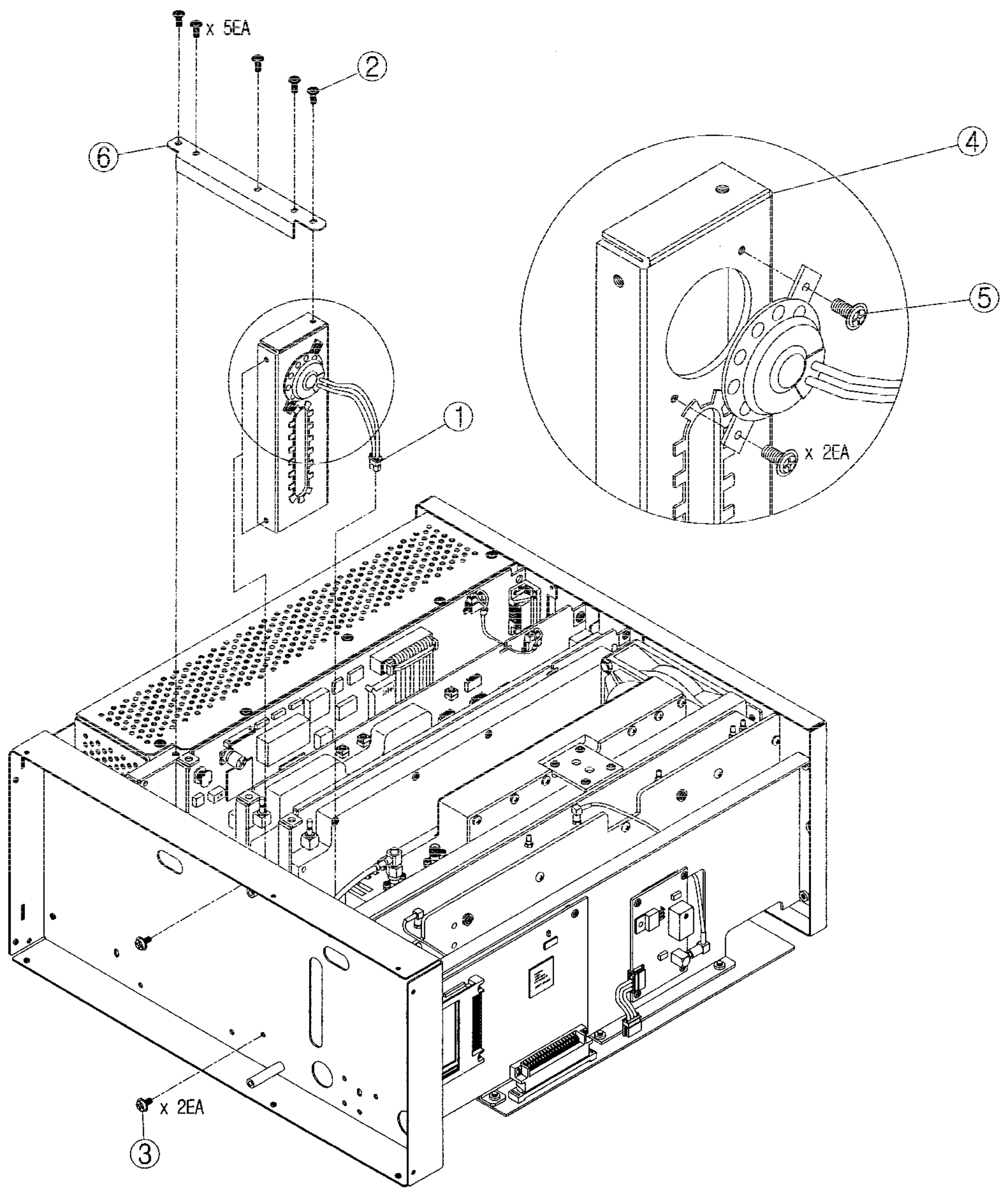

Fig. 5-3-15 SPEAKER ASSEMBLY
(637-021-A)

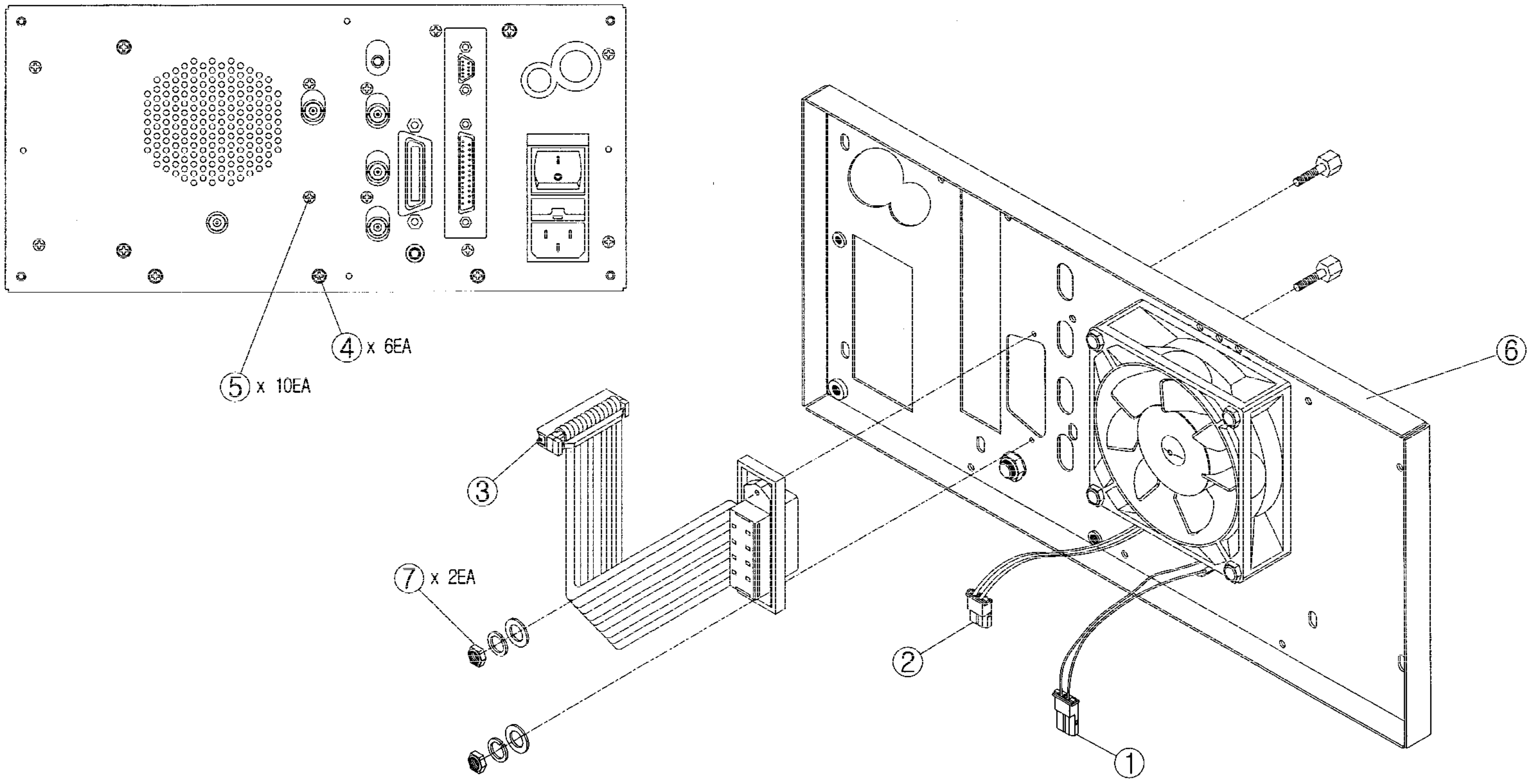

Fig. 5-3-16 GPIB ASSEMBLY
(511-657-A)

GPIB Interface Assembly

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP **PROCEDURE**

1. Remove wire harness ① and ②.
2. Remove wire harness ③.
3. Remove six screws ④ and ten screws ⑤.
4. Remove rear frame assembly ⑥.
5. Remove two nuts ⑦.
6. Remove the assembly as shown.

PCMCIA Board Assembly (Option)

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP	PROCEDURE
1.	Remove three screws ①.
2.	Remove the assembly from the side as shown.

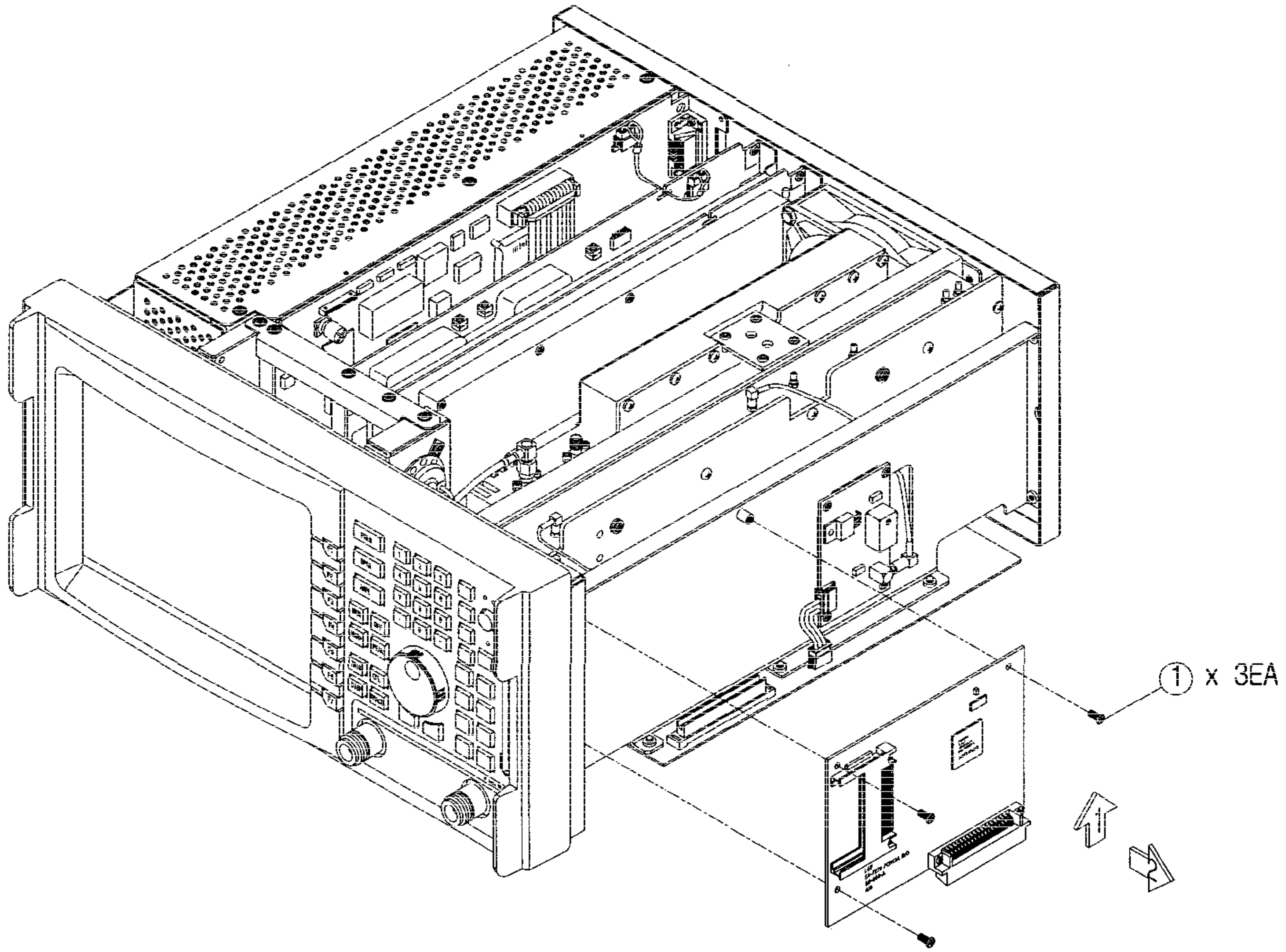

Fig. 5-3-17 PCMCIA BOARD ASSEMBLY (OPTION)
(511-650-A)

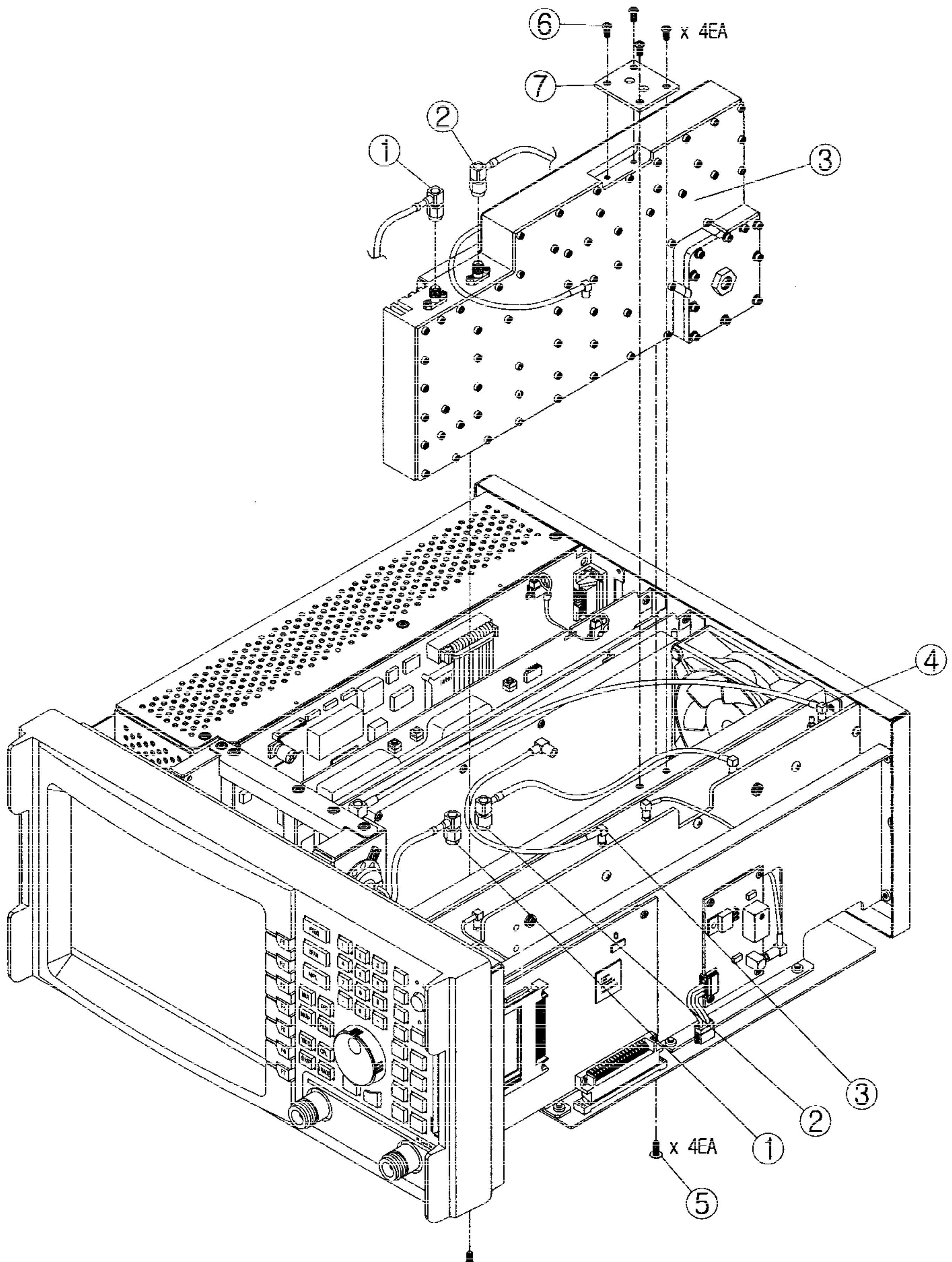

Fig.5-3-18 TRACKING GENERATOR MODULE ASSEMBLY (OPTION)
(636-0031-A)

Tracking Generator Module Assembly (Option)

Preliminary Procedure: Remove Rear Panel Assembly (p. 5-9)

Remove Can Cover Assembly (p. 5-10)

STEP **PROCEDURE**

1. Remove RF cables ① ② ③ (which connect to RF Module assembly).
2. Remove RF cable ④ (which connects to RF Module assembly).
3. Turn the 2398 over and remove two screws ⑤.
4. Remove four screws ⑥ and bracket ⑦.
5. Remove Tracking Generator Module from the top as shown.

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Section 6

Preventive Maintenance

SECTION 6
PREVENTIVE MAINTENANCE

TABLE OF CONTENTS

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SECTION
PREVENTIVE MAINTENANCE

External Cleaning

CAUTION :DISCONNECT POWER FROM TEST SET TO AVOID POSSIBLE DAMAGE TO ELECTRONIC CIRCUITS.

STEP	PROCEDURE

1. Clean front panel, switches and display face with soft lint-free cloth. If dirt is difficult to remove, dampen cloth with water and liquid detergent.
2. Remove grease, fungus and ground-in dirt from surface with soft line-free cloth dampened(not wet) with denatured alcohol.
3. Remove dust and dirt from connector with soft-bristled brush.
4. Clean cable with soft lint-free cloth.
5. Paint exposed metal surface to avoid corrosion.

Internal Cleaning

CAUTION ⚠

CAUTION: DO NOT MOVE COMPONENTS ON CIRCUIT BOARD OR DISASSEMBLE CONNECTORS NEEDLESSLY TO AVOID POSSIBLE DAMAGE.

DO NOT OPEN COMPLEX INTERNAL MODULES FOR SOLE PURPOSE OF CLEANING AND INSPECTION.

PREVENTIVE MAINTENANCE PROCEDURES FOR THE UNIT REQUIRING REMOVAL OF CASE ASSEMBLIES SHOULD ONLY BE PERFORMED IN AN ESD ENVIRONMENT AND ALL PERSONNEL PERFORMING THE PROCEDURES SHOULD HAVE KNOWLEDGE OF ACCEPTED ESD PRACTICES AND/OR BE ESD CERTIFIED.

STEP	PROCEDURE

1. Remove dust with hand-controlled dry air jet of 15psi (1.054kg/cm^2) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.
2. Clean switches and controls with contact cleaner.

Visual Inspection

STEP	PROCEDURE

1. Inspect Chassis for :
   - Tightness of sub-assemblies and chassis mounted connectors.
   - Corrosion or damage to metal surfaces.

2. Inspect Capacitors for :
   - Loose mounting, deformities or obvious physical damage.
   - Leakage or corrosion around leads.

3. Inspect Connectors for :
   - Loose or broken parts , cracked insulation bad contacts.

4. Inspect Circuit Board for :
   - Corrosion or damage to connectors.
   - Damage to mounted components including crystals and ICs.
   - Freedom from foreign material.

5. Inspect Resistors for :
   - Cracked, broken, charred or blistered bodies.
   - Loose or corroded soldering connections.

6. Inspect Semiconductors for :
   - Cracked, broken, charred or discolored bodies.
   - Seals around leads being in place and in good condition.

7. Inspect Wiring for :
   - Broken or loose ends and connections.
   - Proper dress relative to other chassis parts.

   Note : Verify laced wiring is tight with ends securely tied.

PROCEDURE FOR CHANGING THE MEMORY BACKUP BATTERY

The battery mounted on the processor board is used as the power source for backup of system information and calibration data stored in SRAM. The useful life of the battery is approximately 7 years. Should the battery need to be replaced, follow the procedure below.

CAUTION

The procedure for the changing the memory backup battery should be performed using the following steps. Please take care when carrying out this procedure since malfunctions of the 2398 may occur if these steps are not correctly performed.

Replacement battery: Sanyo CR 12600SE-FT3.   IFR part number 649-013.

Procedure

1. Back up (upload) the factory calibration data of the system to the PC as a file according to the 'Calibration Data Backup Procedure' on page 3-29 (the data stored in the system will be erased completely when the backup battery is detached from the processor board). If the 2398 has a PCMCIA option installed, it is recommended that any user setup status stores, trace stores (Trace A and B) and limit stores are backed up on a PCMCIA memory card (see User manual).
2. Check to see if the data was correctly backed up by opening the backup file with the 'memo' program of the PC. Take care not to erase the saved file after changing the battery.
3. Disconnect the 2398 from any power source.
4. Remove the processor board from the 2398 according to the procedure on page 5-22. Take care that the processor board is not be exposed to static electricity.

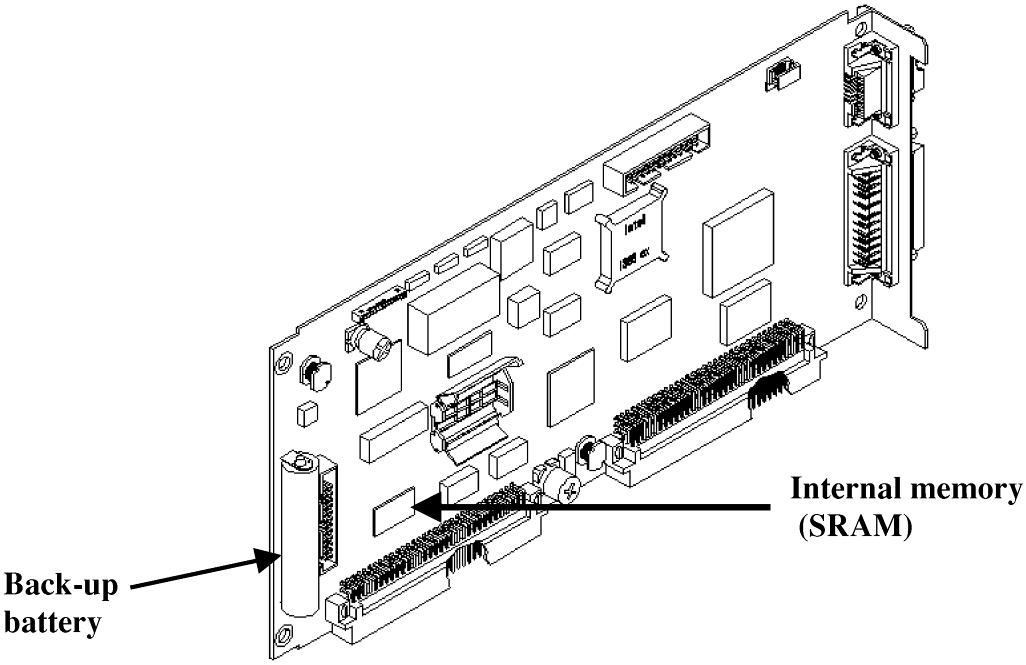


Fig. 6-1 Processor board

5. Detach the battery from the board with a soldering iron and de-soldering braid (solder wick).
6. Insert and solder the new battery onto the PCB. Take care to observe the correct polarity of the battery.
7. Re-install the processor board to the instrument. Take care that the '+' terminal of the battery does not touch the instrument chassis when installing the board.
8. Assemble the system in reverse order to that of disassembly.
9. Connect the 2398 to power source and switch on. Check that the instrument powers up successfully and operates normally.
10. Clear the SRAM memory before restoring the calibration data:
    a. Press the [CONFIG] key in the front panel, the "MORE.." softkey [F7] and the "FACTORY CONFIG.." softkey [F1].
    b. Input the password 27329780.
    c. Choose the "CLEAR CAL.." softkey [F5] and the following sub-menu is displayed:

        [F1]: RBW CLEAR

        [F2]: RX FLAT CLEAR

        [F3]: RX ATT CLEAR

        [F4]: IF ATT CLEAR

        [F5]: LOG AMP CLEAR

        [F6]: SRAM CLEAR

[F7]: RETURN

d. Press each of these softkeys from [F1] to [F7] in order.

e. Move to the higher menu by choosing the last key [F7].

11. Turn the power “off” and then “on” to initialize the memory.
12. Download the calibration data stored in the PC to the 2398 according to the Calibration Data Backup Procedure.
13. Check the data downloaded to the 2398 is correct, as follows:

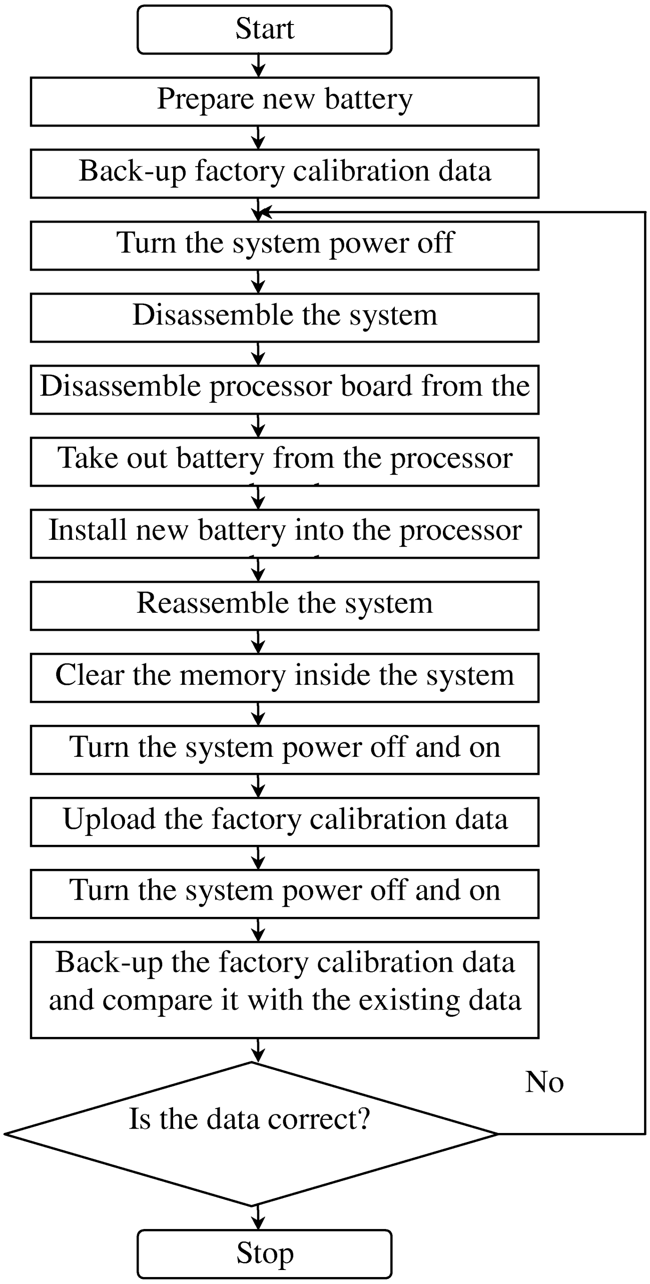
a. Make sure the system power is “off” and then turn it “on”.

b. Back up (upload) the factory calibration data of the 2398 to the PC as a different file name to that previously used in step 1.

c. Compare the file created in step 13.b with that in step 1. If the two files are the same, the battery change has been correctly completed.

14. If the two files are different, repeat the steps 12 and 13. If they are still different after the steps are repeated, the battery change was incorrectly performed. In this case repeat steps from 3 to 13.

Flow diagram for changing the memory backup battery



Section 7

Parts List

SECTION 7
PARTS LIST

TABLE OF CONTENTS

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SECTION 7
PARTS LIST

GENERAL

This section contains the part numbers and description for replaceable part and assemblies in the 2398 Spectrum Analyzer.

LIST OF 2398 ASSEMBLIES

Can Cover Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	219-248I	CAN COVER
02	222-001IR1	STAND
03	242-329	HANDLE PLATE
04	318-002I	HANDLE
05	375-034I	HANDLE CAP
06	377-008I	STAND FOOT
07	377-009R1	DOWN FOOT
08	MBC03P06J	B/H SCREW, NASALOK, M3X6
09	MCC0408J	C'S/H SCREW, NASALOC, M4X8
10	WPL3-10	PLAIN WASHER
11	375-035I	RUBB-FOOT CAP
12	377-012I	RUBBER FOOT-R
13	377-012I-1	RUBBER FOOT-L

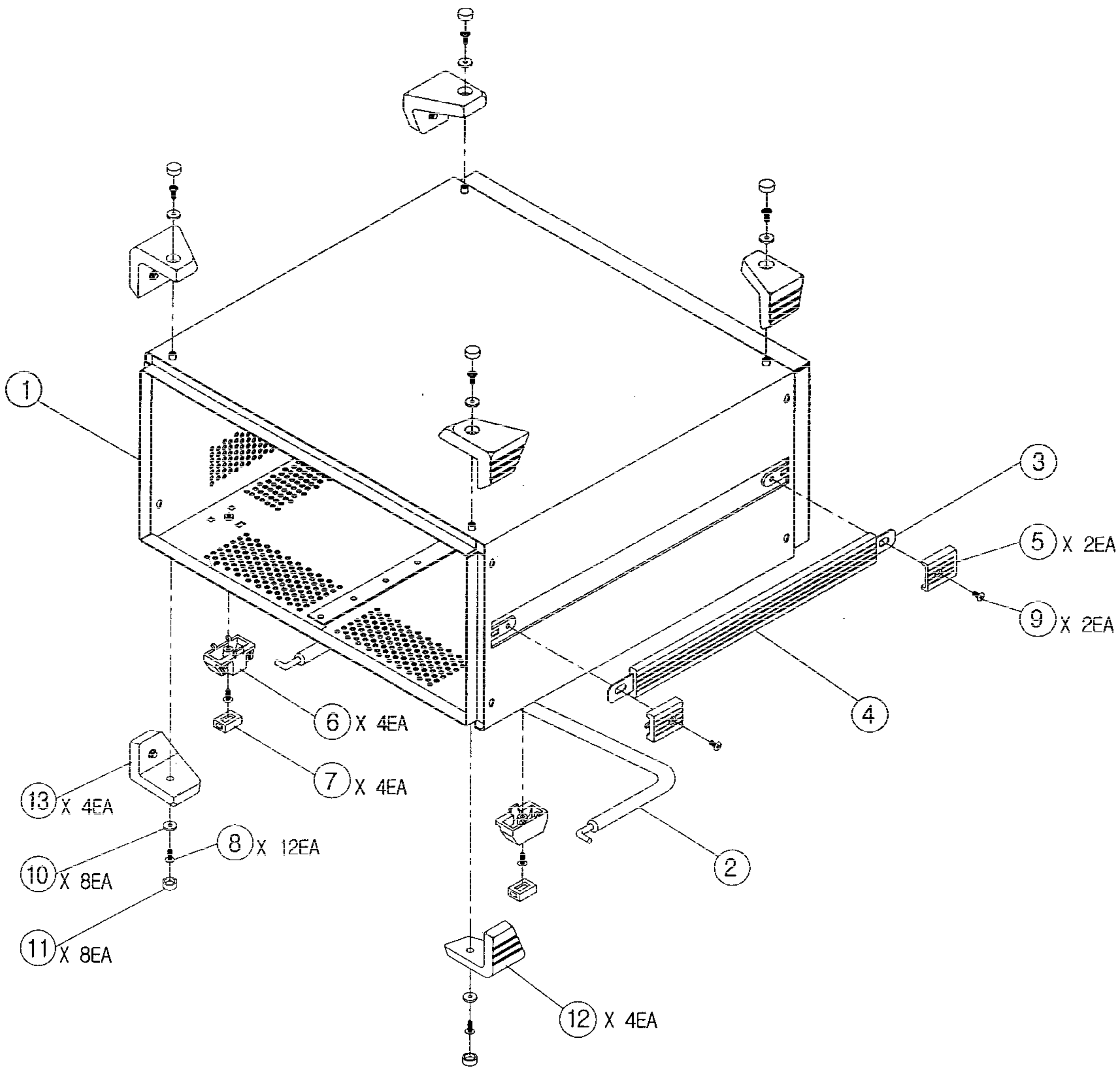

Fig. 8-2-1 CAN COVER ASSEMBLY
(217-1741-A)

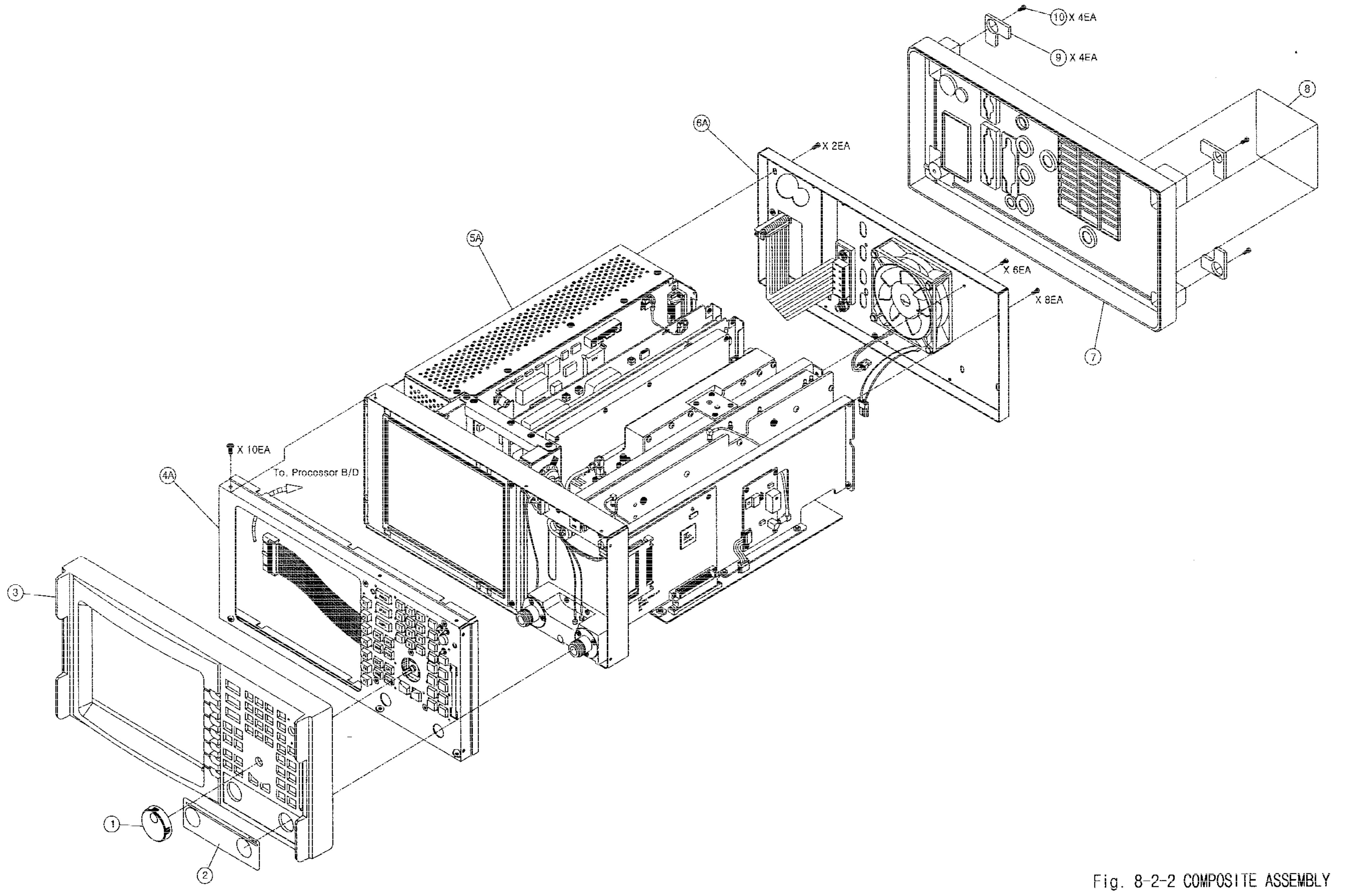

Fig. 8-2-2 COMPOSITE ASSEMBLY

Composite Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	369-218IR3	ENCODER KNOB
02	277-717IR1	RF INPUT LABEL (WITH TRACKING GEN)
OR	277-717IR3	RF INPUT LABEL (WITHOUT TRACKING GEN)
03	247-174IR2	FRONT PANEL
04A	212-003I-A	FRONT FRAME ASSEMBLY
05A	221-065I-A	MAIN BODY ASSEMBLY
06A	227-114-A	REAR FRAME ASSEMBLY
07	274-175IR3	REAR PANEL
08	273-111IR1	STICKER, SERIAL NO.
09	377-010R1	FOOT REAR
10	MBC04P08J	SCREW, M4X8

Front Frame Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	227-110R1	FRONT FRAME
02	360-039IR1	RUBBER KEY-PAD
03	511-634-A	KEYBOARD ASSEMBLY
04	MBC03P06J	SCREW, M3X6

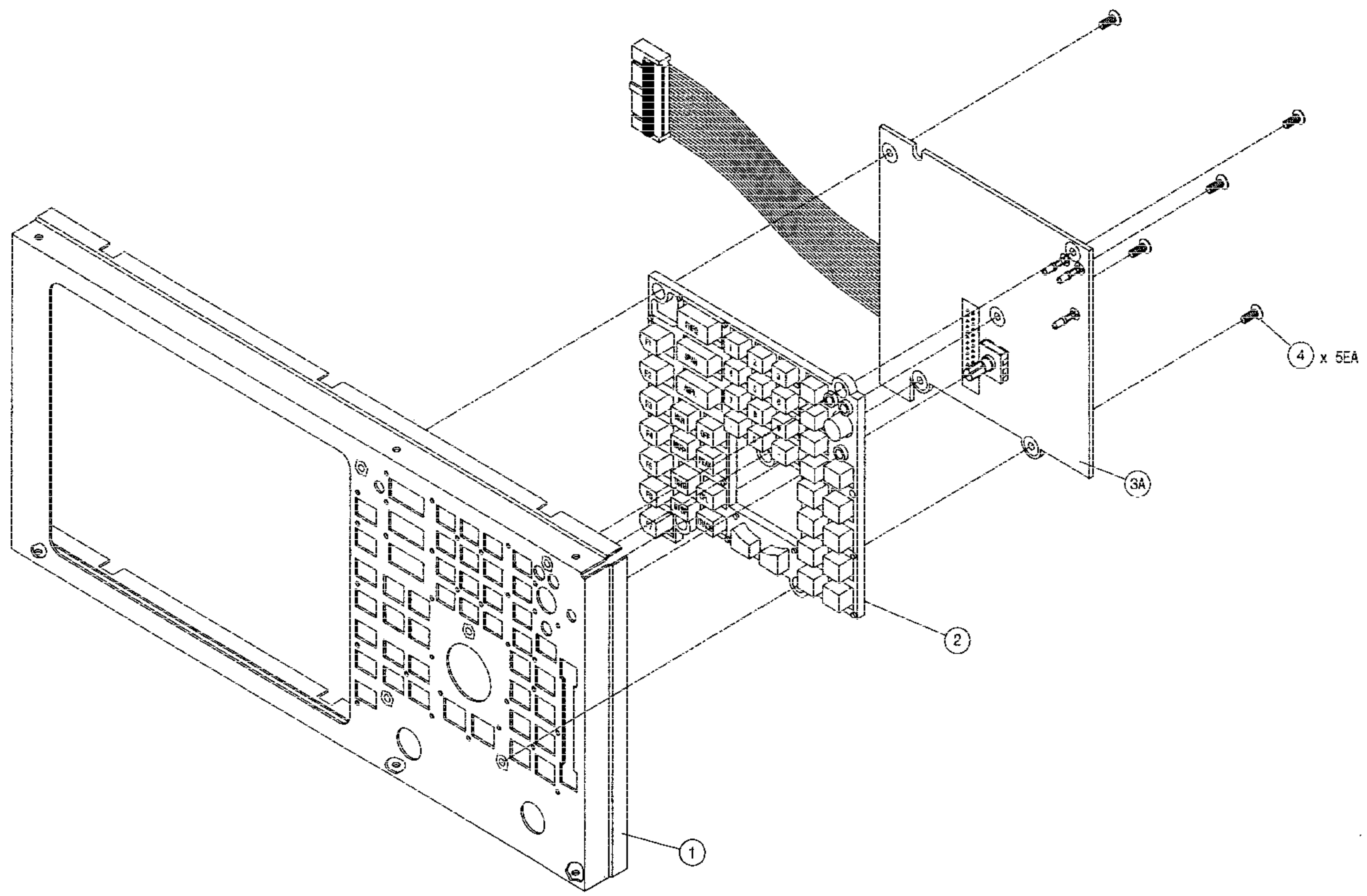

Fig. 8-2-2-1 FRONT FRAME ASSEMBLY
(212-0031-A)

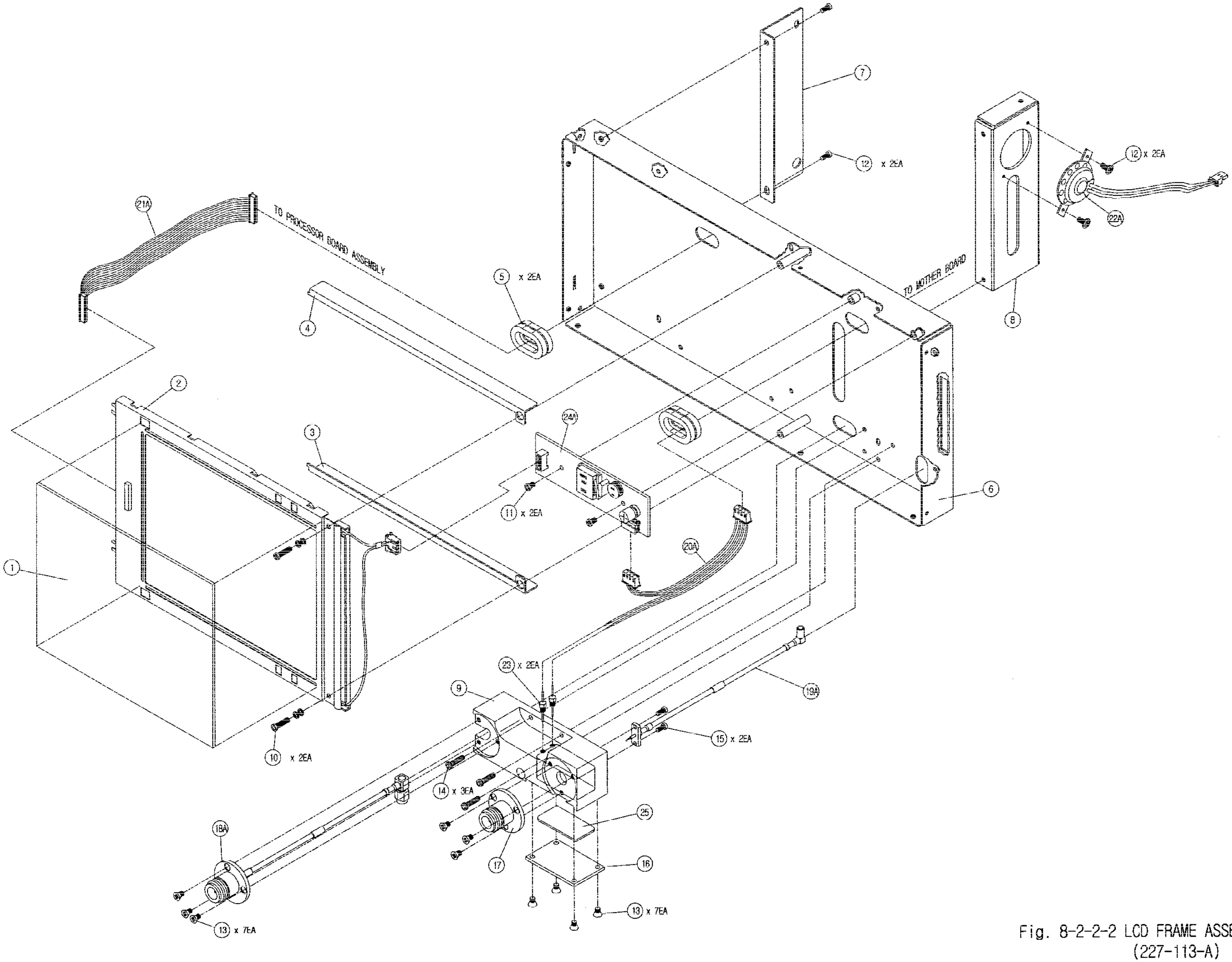

Fig. 8-2-2-2 LCD FRAME ASSEMBLY
(227-113-A)

LCD Frame Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	249-270R1	LCD WINDOW
02	588-066	LCD, LM64P101/SHARP
03	235-273-1	LCD SUPPORT, BRAKET-T
04	235-273-2	LCD SUPPORT, BRAKET-B
05	353-073	GROMMET, NEOPREN
06	227-113	LCD FRAME
07	235-272	POWER SUPPLY BRAKET
08	235-274	PCB SUPPORT BRAKET
09	265-031-1R1	BLOCK, RF INPUT
10	MPC03A16J	SCREW, M3XL16
11	MBC03P06J	SCREW, M3XL6
12	MBT03C06B	SCREW, TAPTITE, M3XL6
13	MCC03-05P-2	SCREW, C'S HEAD, M3XL5
14	MPC03B10P	SCREW, M3XL10
15	MPC25B06P	SCREW, M2.5XL6
16	219-264	COVER, RF INPUT BLOCK
17	531-551	CONN, RF INPUT, N-21J-GO-21
18	550-926-A	CABLE ASSEMBLY, TG-OUT
19	550-920-A	CABLE ASSEMBLY, RF INPUT
20	550-922-A	W/H9, LCD INVERTER TO MOTHER
21	550-906-A	W/H1, LCD TO PROCESSOR BOARD
22	639-021-A	SPEAKER ASSEMBLY
23	581-294	CAPACITOR, DFT301-801X7R103S50M
24	511-647-A	LCD INVERTER B/D ASSEMBLY

Main Body Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	227-113	LCD FRAME
02A	235-274-A	PCB SUPPORT BRAKET ASSEMBLY
04	227-111	MAIN FRAME
05	227-112	MID FRAME
06	235-270	FIXING BRACKET
07	235-272	POWER SUPPLY BRACKET
08	235-285	TG MOUNTING BRACKET (OPTION)
09	MBT03C06B	SCREW, TAPTITE, M3XL6
10	MBC03P06J	SCREW, M3XL6
11	MPC03A40J	SCREW, M3XL40
12	MPC03B06P	SCREW, M3XL6
13	MPC03P08J	SCREW, M4XL8
14A	7005-2640-500	RF MODULE ASSEMBLY
15	511-648-A	IF FILTER & AMP ASSEMBLY
16	511-648-A	VIDEO DETECTOR B/D ASSEMBLY
OR	511-706-A	*VIDEO DET B/D WITH QUASI-PEAK ASSY
17	511-649-A	PROCESSOR B/D ASSEMBLY
20	516-003-A	AC POWER SUPPLY MODULE
21A	636-003-A	*TRACKING GENERATOR ASSEMBLY
22	511-660-A	MSO B/D ASSEMBLY
23	511-650-A	*PCMCIA B/D ASSEMBLY
24	511-645-A	MOTHER B/D ASSEMBLY
25	550-916-A	W/H, MSO B/D TO MOTHER B/D

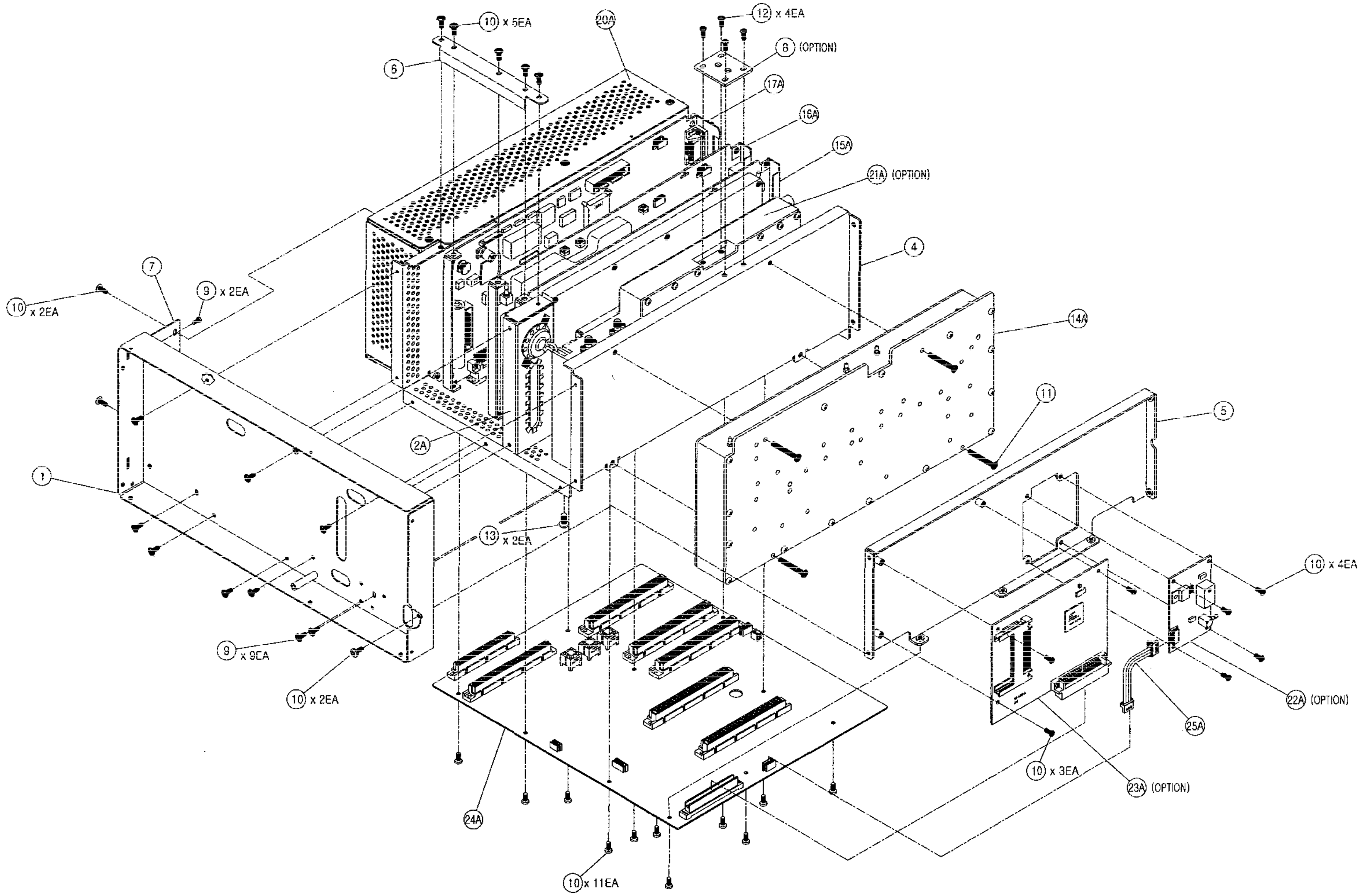

Fig. 8-2-2-3 MAIN BODY ASSEMBLY
(221-0651-A)

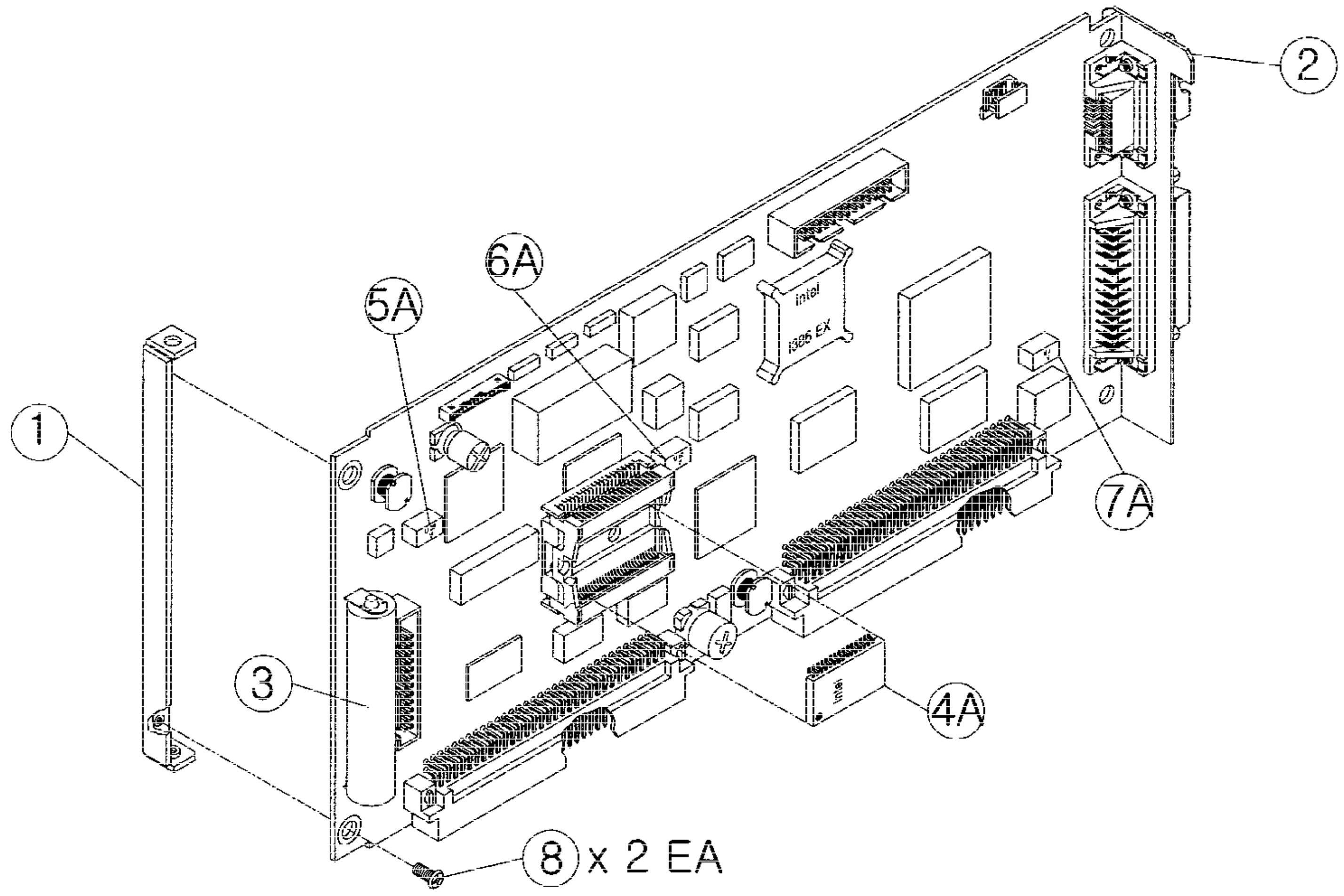

Fig. 8-2-2-7 PROCESSOR BOARD ASSEMBLY
(511-646-A)

Processor Board Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	235-275	PROC FRONT, 2398
02	235-276	PROC REAR, 2398
03	649-013	BATTERY, CR12600SE-FT3 SANYO
04	597-028-A	PROGRAMMED IC, 2398, INTEL

Rear Frame Assembly

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
01	227-114	REAR FRAME
02	531-164R2	CONN, BNC, UG-1094/U
03	537-018	TERMINAL, Z.048
04	511-657-A	*GPIB ASSEMBLY
05	550-912-A	W/H9, REAR BNC TO MOTHER
06	639-010-A	DC FAN ASSEMBLY
07	NHB04-00J	NUT, HEX M4

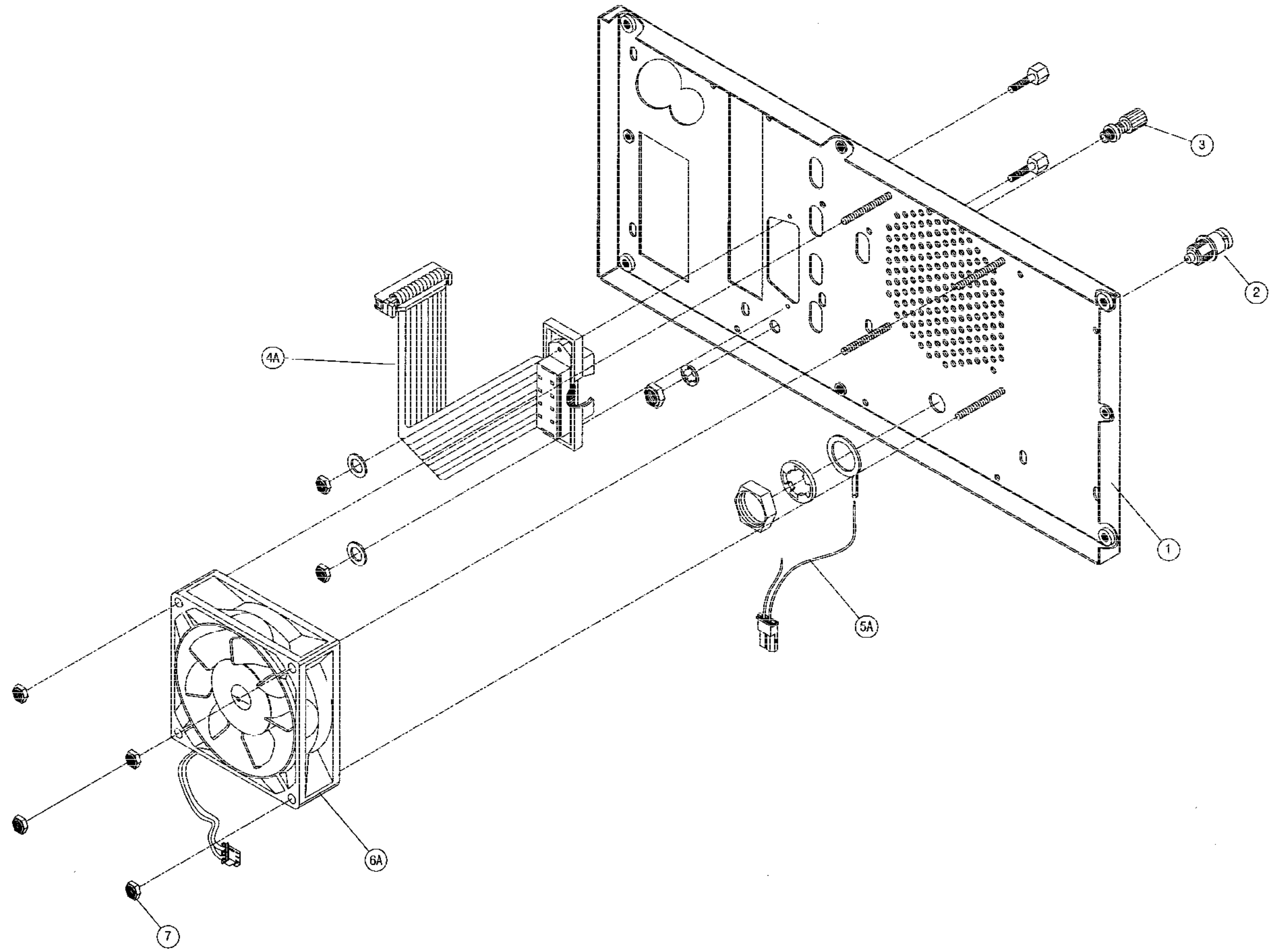

Fig. 8-2-2-9 REAR FRAME ASSEMBLY
(227-114-A)

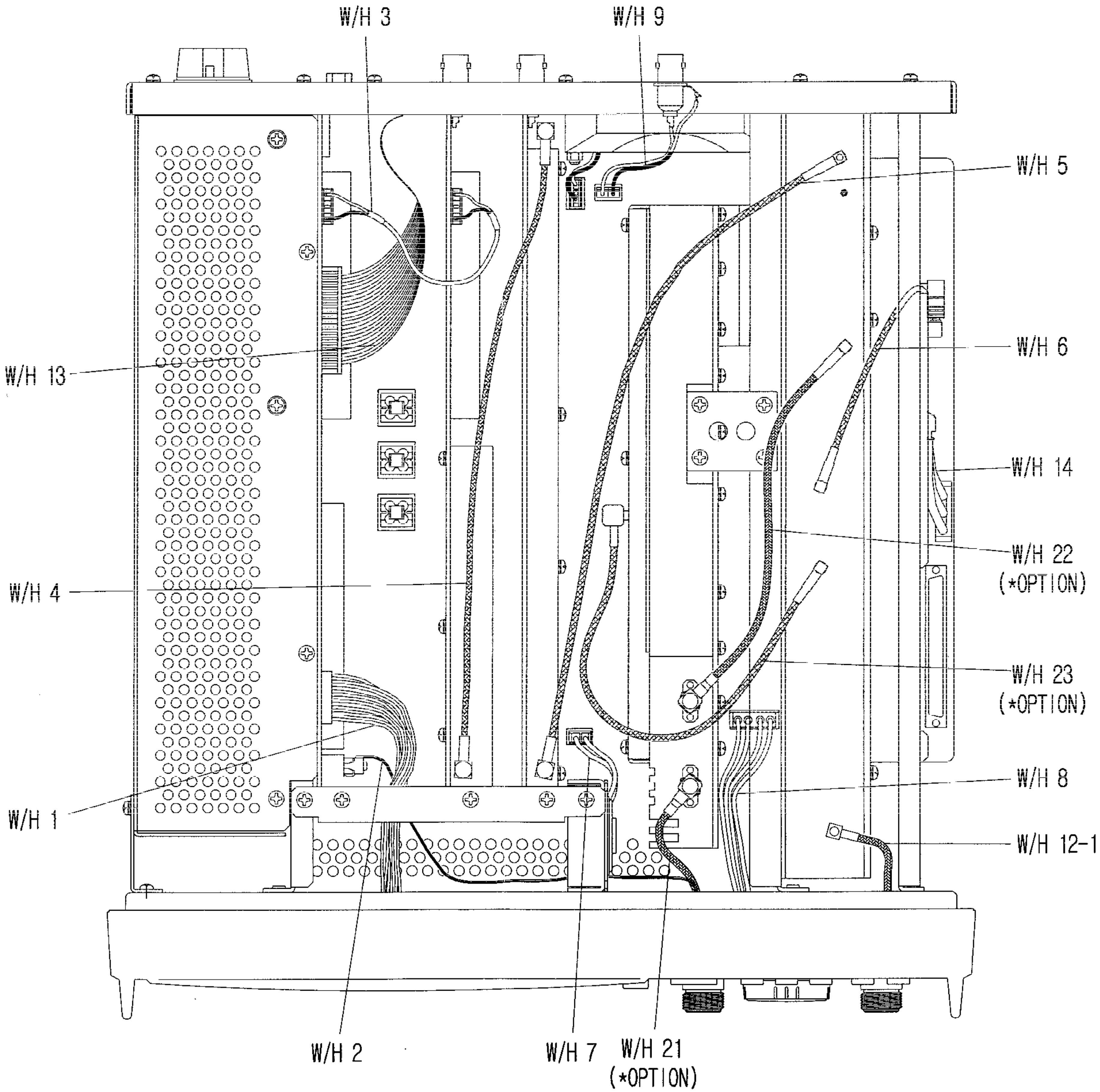

Fig. 8-2-3 COMPOSITE ASSEMBLY(W/H)

Wire Harness

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
W/H1	550-906-A	LCD TO PROCESSOR
W/H2	550-914-A	KEY B/D TO PROCESSOR
W/H3	550-907-A	VIDEO TO PROCESSOR
W/H4	550-908-A	IF TO VIDEO
W/H5	550-909-A	RF TO IF
W/H6	550-915-A	MSO TO RF
W/H7	550-910-A	SPEAKER ASSEMBLY
W/H8	550-922-A	LCD INVERTER TO MOTHER
W/H9	550-912-A	10M EXT. OUT TO MOTHER
W/H12	550-920-A	RF INPUT
W/H13	550-917-A	*GPIB TO PROCESSOR (OPTION)
W/H14	550-916-A	MSO/*HSO (OPTION) TO MOTHER
W/H22	550-924-A	*RF YIG OUT TO TG (OPTION)
W/H23	550-925-A	*RF 80MHz TO TG (OPTION)

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Appendix

APPENDICES

TABLE OF CONTENTS

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APPENDICES

User I/O Connectors and Pin-Out Tables

CONNECTOR	TYPE	IN/OUT	SIGNAL
AC Input	IEC 320 Socket	Input	AC Power
RF Input	Type N Female	Input	RF
Optional tracking generator Output	Type N Female	Output	RF
External trigger output	BNC Female	Input	
External sweep gate output	BNC Female	Output	
external video output	BNC Female	Output	
External Reference Oscillator IN/OUT	BNC Female	IN/OUT	IN: 10 MHz OUT:10 MHz
IF Output	BNC Female	Output	10.7 MHz
IEEE-488 GPIB	24-Pin Champ	IN/OUT	See Pin-Out (table 2).
Printer	25-Pin, D-sub Female	Output	See Screen Print Data, Pin-Out(table 4).
RS-232C	9-Pin, D-sub Male	IN/OUT	See Pin-Out (table 3).

TABLE A-1. I/O CONNECTORS

IEEE-488 GPIB Connector

The IEEE-488 GPIB connector complies with ANSI/IEEE standard 488.2-1987.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EQI	17	REN
6	DAV	18	Ground
7	NRFD	19	Ground
8	NDAC	20	Ground
9	IFC	21	Ground
10	SRQ	22	Ground
11	ATN	23	Ground
12	Ground	24	Ground

Table A-2. Pin-Out for IEEE-488 GPIB connector

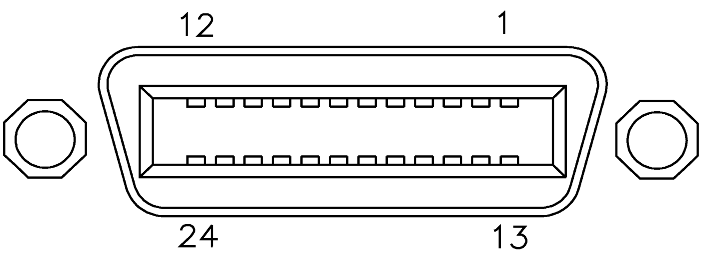

Figure A-1. IEEE-488 GPIB Connector

RS-232 CONNECTOR

PIN NUMBER	SIGNAL
1	DCD
2	RXD
3	TXD
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	R1(NC)

Table A-3. Pin-Out for RS-232C Connector

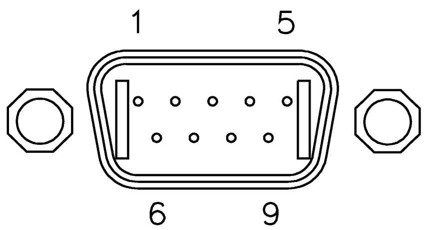

Figure A-2. RS-232C Connector

PRINTER CONNECTOR

PIN NUMBER	SIGNAL
1	$\overline{\text{STB}}$
2	PD0
3	PD1
4	PD2
5	PD3
6	PD4
7	PD5
8	PD6
9	PD7
10	$\overline{\text{ACK}}$
11	BUSY
12	PE
13	SLCT
14	$\overline{\text{AFD}}$
15	$\overline{\text{ERROR}}$
16	$\overline{\text{INIT}}$
17	$\overline{\text{SLIN}}$
18	Ground
19	Ground
20	Ground
21	Ground
22	Ground
23	Ground
24	Ground
25	Ground

Table A-4. Pin-Out for PRINTER Connector

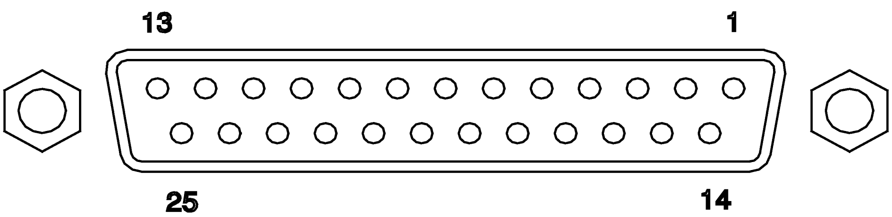

Figure A-3. PRINTER Connector

DC INPUT CONNECTOR(Option)

PIN NUMBER	SIGNAL
1	LED-Anode
2	Battery +
3	Battery +
4	Battery +
5	Battery -
6	Battery -
7	LED-Cathode
8	Battery -

TableA-5. Pin-Out for DC Input Connector

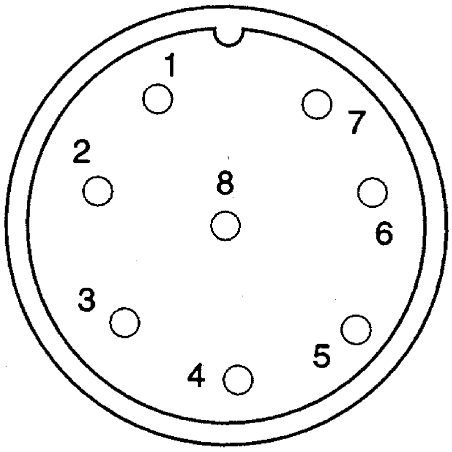

Figure A-4. DC Input Connector(Front View)

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